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THESIS

THE DESIGN AND IMPLEMENTATION OF A
DIGITALLY PROGRAMMABLE GIC FILTER

by

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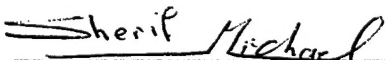
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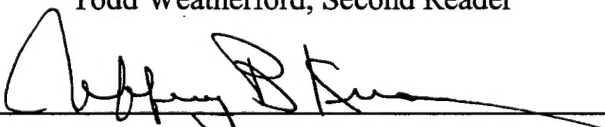## NAVAL POSTGRADUATE SCHOOL
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ABSTRACT

In this research, the design and implementation of an integrated-circuit, digitally programmable, analog-to-analog filter are presented. By functioning in the analog domain the quantization errors and hardware requirements of analog-to-digital, and digital-to-analog, conversion are eliminated. The filter design of this project utilizes switched-capacitors and the Generalized Immitance Converter to eliminate resistors and inductors. The resulting design is therefore suitable for fabrication by modern integrated-circuit technology. The design also features digital programmability, so that the filter can easily interface with modern digital systems. The overall filtering circuit is programmable in filter topology, quality factor, and cutoff (or center) frequency, making it useful in a wide range of applications.

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I. INTRODUCTION

A. BACKGROUND

Most electronic systems require some degree of signal filtering or conditioning in order to function properly. In the early 1960's most electronic filters were constructed using discrete analog components, such as resistors, capacitors, and inductors. These systems were often complex, difficult to produce, sensitive to individual component variations, and very costly. As circuit technology progressed digital systems began to provide designers with smaller, lighter, and faster functionality. Today digital systems are the forefront of most electronic systems. Currently there is a great deal of focus on *Digital Signal Processing* (DSP) to provide the required signal filtering or conditioning. However, the emergence of digital technology has not obviated analog systems. The world we live in is an analog system. Therefore, circuit designers will always have to deal with analog signals in some way. There are numerous electronic systems in which input and output signals are analog in nature. In such systems Digital Signal Processing requires analog-to-digital signal conversion prior to processing, and digital-to-analog conversion after processing. These conversions introduce quantization errors into the signal, increase hardware requirements, and delay circuit response. A filter acting in the analog domain can avoid these conversion errors, and function with reduced hardware requirements.

Analog filtering may provide some benefit over DSP, but unless a circuit can be manufactured in *Integrated Circuit* (IC) form, its utility in modern systems is severely limited. Therefore, analog filters constructed of discrete components are of very limited interest. On the other hand, integrated circuit analog filters could prove to be extremely

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useful. While it is technically possible to construct discrete analog components in IC form, modern IC fabrication techniques are not optimized for production of most passive analog components. Therefore, any integrated circuit analog filter design must, in some way, eliminate these problematic components, yet still provide the necessary filtering characteristics.

The research effort of this project seeks to develop an analog-to-analog filter design which is suitable for fabrication by current IC manufacturing techniques, provides high quality programmable filtering, and interfaces with modern digital systems.

B. THESIS ORGANIZATION

Background information, and the basics of electronic filtering are provided in Chapter II. Chapter III discusses the Operational Amplifier – one of the key components of analog filter circuits. Switched Capacitors, a technique used to simulate resistive impedances, are covered in Chapter IV. The basics of the *Generalized Impedance Converter* (GIC) filter, the foundation for the filter design of this project, are discussed in Chapter V. Chapter VI introduces some advanced concepts of the GIC filter, and develops the overall circuit design of this project. The integrated circuit implementation of the filter is covered in Chapter VII. Finally, results and conclusions are outlined in Chapter VIII.

II.   FILTER BASICS

An electrical filter is a device consisting of an interconnection of components, such as resistors, capacitors, inductors, and active devices (transistors, amplifiers, controlled sources). [Ref. 1] The purpose of a filter is to operate on an input electrical signal, the *excitation signal*, and produce an output, *response signal*, which exhibits a modified frequency spectrum. Specifically, a filter is designed to pass or amplify certain portions of a signal's spectrum (certain frequencies), and at the same time block or attenuate other portions of the excitation signal spectrum. "In essence, a filter converts inputs into outputs in such a fashion that certain desirable features of the inputs are retained in the outputs, while undesirable features are suppressed." [Ref. 2] Filters are extremely important in modern electronic systems. In fact, filters permeate modern technology so much that it is difficult to think of an electronic system which does not utilize a filter in some way. [Ref. 3]

When designing or selecting a filter for use in a circuit one must determine the frequency selection characteristics of the filter in order to meet requirements. In general filters are separated into several categories based upon the shape of their frequency response. The next section will introduce and discuss these categories.

A.   FILTER TYPES

The interest in, and indeed the utility of, filters lies in their performance of frequency selective functions: passing signals whose frequency spectrum lies within a specified range, and stopping signals whose frequency spectrum falls outside this range. Such filters ideally have frequency bands over which the magnitude of transmission is unity or greater (the filter *passband*) and frequency bands over which the transmission is

zero (the filter *stopband*). [Ref. 4] Generally there are considered to be four major types of filters: low-pass (LP), high-pass (HP), band-pass (BP), and band-stop (BS) or notch (N). Table 2.1 illustrates these basic filter types, showing their respective ideal frequency response.
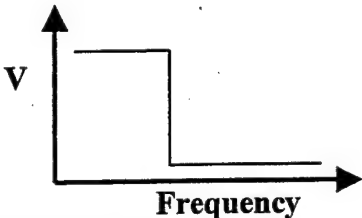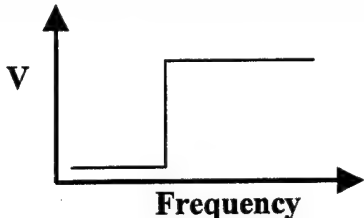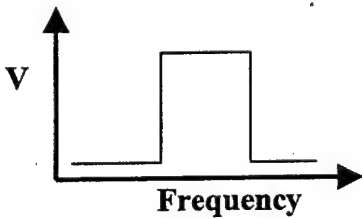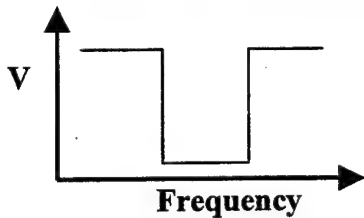
Lowpass	Highpass
Bandpass	Notch

Table 2.1: Ideal Frequency Response of the Four Basic Filter Types

The filter frequency responses illustrated in Table 2.1, like most ideal representations, are not physically realizable. Rather, real filters exhibit *transition bands* in which the frequency response varies from the passband response to the stopband response. The width of these transition bands determines the "sharpness" of the filter response, and its selectivity. Table 2.2 illustrates typical non-ideal frequency responses

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for the four basic filter types, along with a basic circuit network which can be used to realize each filter type.
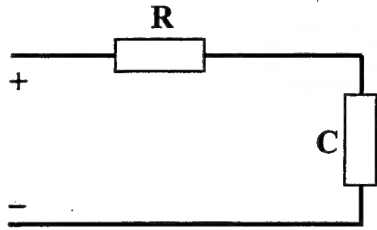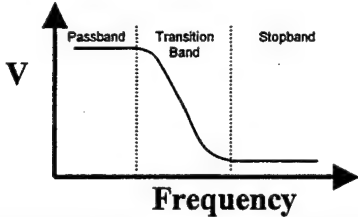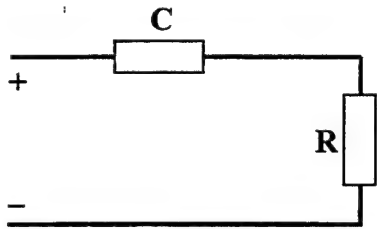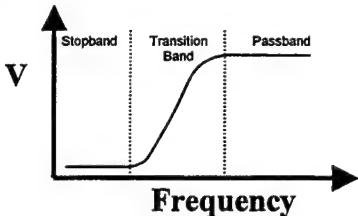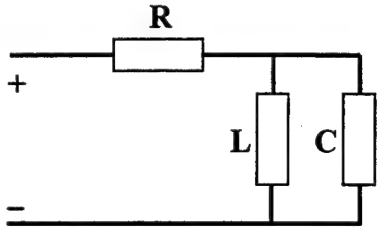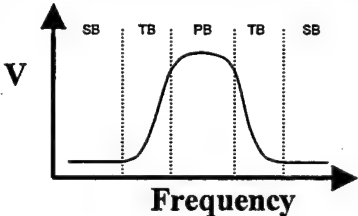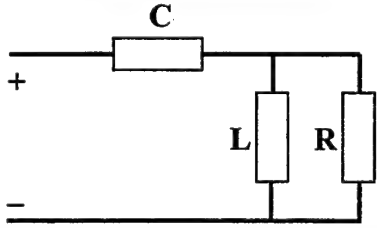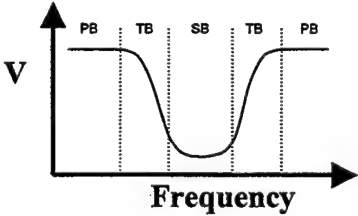
RC Low-Pass Filter	Non-Ideal Response
RC High-Pass Filter	Non-Ideal Response
RLC Band-Pass Filter	Non-Ideal Response
RLC Notch Filter	Non-Ideal Response

Table 2.2: Four Basic Filter Types with Corresponding Non-Ideal Frequency Responses

Generally filters are specified by using a transfer function. In order to achieve all of the basic filter types the transfer function must be at least second order. Table 2.3 shows the form of the transfer function for each of the various filter types. The cutoff or center frequency of each filter is given by ω_p, while the quality factor is given by Q_p, and the value a_i is a constant.

Filter Type	Transfer Function
Low-Pass	$T(s) = \dfrac{a_0}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
High-Pass	$T(s) = \dfrac{a_2 s^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Band-Pass	$T(s) = \dfrac{a_1 s}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Notch	$T(s) = \dfrac{s^2 + \omega_p^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$

Table 2.3: Transfer Functions of the Four Basic Filter Types

The ability of the GIC filter to realize the transfer function of any of the basic filter types will be shown in Chapter V.

B.   FILTER SELECTIVITY

The issue of selectivity is an important one. Obviously one would like a filter which exhibits maximum frequency selectivity. During design the more tightly one specifies a filter the closer the response is to the ideal of maximum selectivity. However, the resulting filter circuit must be of higher order and thus more complex and expensive to implement. [Ref. 4] Filter selection is then, like many aspects of circuit design, a compromise. One must select and specify a filter which exhibits enough selectivity to function properly in the overall circuit, yet one must also select a filter design which is not prohibitively complex or expensive.

The sharpness, or selectivity, of the filter is usually referred to as the *quality factor Q*. [Ref. 5] In many filters the quality factor is an important parameter. This is especially important in band-pass filters, which often are used to pass only a very narrow band of frequencies. [Ref. 6] Figures 2.1 and 2.2 illustrate the quality factor for low-pass and band-pass filters.
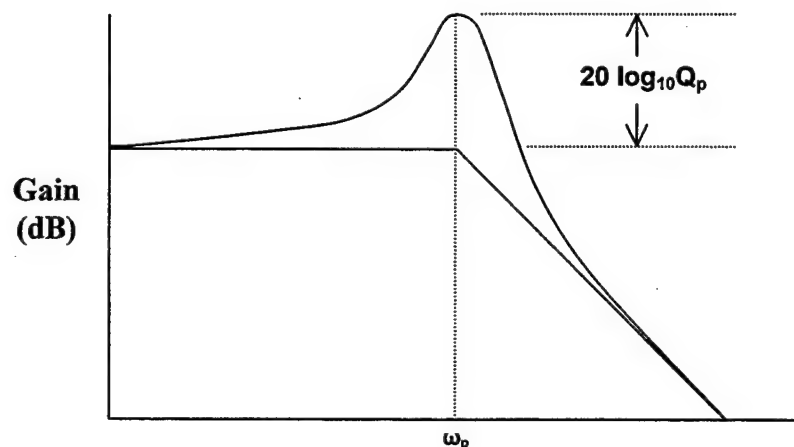
Figure 2.1: Q-Factor of Low-pass Filter

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$$Q_p = \frac{\omega_p}{\omega_2 - \omega_1}$$
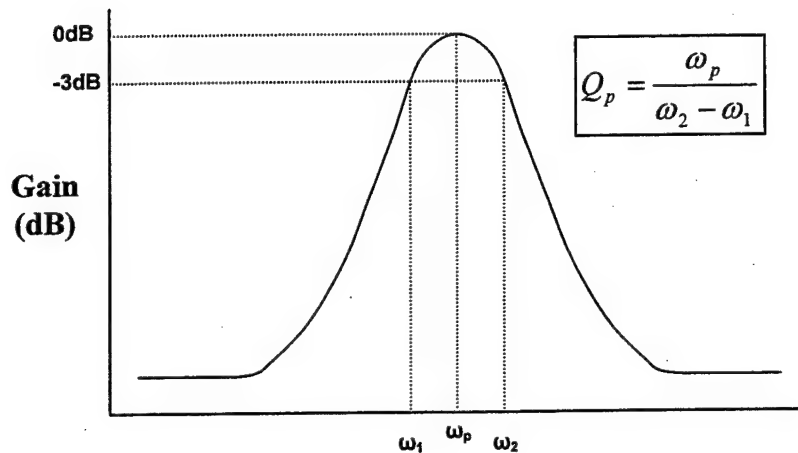
Figure 2.2: Q-Factor of Bandpass Filter

Often time the quality factor of a filter will determine what applications it is appropriate for, and its usefulness in general. Thus, any filter design project must include a specification of the quality factor. Additionally, if the filter is variable or programmable in frequency it is also extremely useful if it is variable in Q-factor as well.

C.   THE GIC FILTER

Having discussed some of the basic topics relevant to filters in general, we may now turn our attention to the project at hand. Filters are designed in various configurations in order to suit specific applications, or to exploit certain characteristics. In an attempt to maximize its utility the overall filter of this project will be programmable in topology (filter type), frequency, and quality factor. Such a filter design will have usefulness in a wide range of applications.

In order to realize all possible filter types it is generally necessary for a circuit to contain impedances of all three passive types (resistors, inductors, and capacitors).

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However, it will be shown that integrated circuit manufacturing of resistors and inductors is wrought with difficulty, exhibits poor tolerances, is prohibitively expensive, and is, as a result, not suitable for large scale implementation. The use of active components, switched capacitor networks, and the *Generalized-Immitance (or Impedance) Converter (GIC)* design will allow for the elimination of resistors and inductors by simulating their respective impedances. Additionally, digital circuit technology will allow for digital programmability of the entire circuit. Chapter III will deal with Operational Amplifiers, one of the crucial active components in the circuit. Chapter IV will introduce Switched Capacitor networks, the means by which we can eliminate resistors from the circuit. Chapter V will introduce the GIC filter design. This design will allow us to simulate inductors, and achieve a circuit which is programmable in topology (type), frequency, and quality factor.

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III. OPERATIONAL AMPLIFIERS

A. INTRODUCTION

The operational amplifier, commonly referred to as the op amp, is designed to function as a differential amplifier with an extremely high open-loop gain and bandwidth. In the ideal cases both the gain and bandwidth are treated as being infinite. The op amp is one of the most versatile building blocks in linear circuit applications, and is an extensively used component in analog circuit design. [Ref. 4, 5] In fact, it has been pointed out that "one can do almost anything with op amps". [Ref. 3]

Early op amps were constructed of discrete components, and were prohibitively high in cost, while exhibiting poor performance characteristics. In the mid-1960's Fairchild Semiconductor introduced the first integrated circuit (IC) op amp. [Ref. 3, 6] This first integrated circuit op amp, designated the μA 709, signaled a new era in electronic circuit design. With the new availability of IC op amps circuit designer began to use them in ever greater quantities. This in turn led to a reduction in cost, and increases in performance. Soon after the μA 709 came the μA 741, a workhorse op amp whose basic design is still in use today. With the advent of the highly successful μA 741, op amps became an almost ubiquitous part of electronic circuitry.

Inevitably design variations of the μA 741 were created in efforts to improve on certain performance characteristics. Today there are numerous general and special purpose op amps for designers to choose from. What has not changed is the general usefulness and importance of these devices. The op amp is a critical portion of the design of any analog or sampled data circuit. For this reason the next section will examine some of the important characteristics and parameters of op amps.

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B. OPERATIONAL AMPLIFIER CHARACTERISTICS

This section will introduce and define some of the key parameters of operational amplifiers. Where appropriate, values of these parameters for the theoretical ideal op amp will be given. In general the real op amp is a device which performs relatively well when compared to the ideal. However, certain crucial limitations imposed by real world op amp characteristics will dictate the design and function of overall circuit of this project.

1. Open-loop Gain
Figure 3.1 shows the circuit symbol for an op amp.
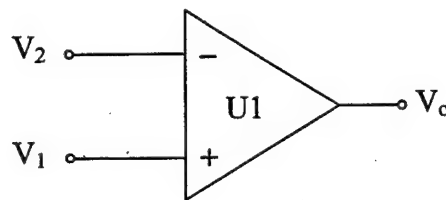
Figure 3.1: Op Amp Circuit Symbol

The open-loop gain of the op amp, A, is defined by the equation

$$V_o = A(V_1 - V_2) \Rightarrow A = \frac{V_o}{(V_1 - V_2)} \qquad \text{(Eq. 3.1)}$$

The ideal op amp should have a gain whose value is very large and ideally infinite $A_{ideal} = \infty$. An infinite gain is, however, not physically realizable. A real op amp has a finite gain. The typical values for op amp gain range from 100 to 10^6.

2. Frequency Response / Bandwidth
One of the most important characteristics of an op amp is its frequency response. In the ideal case the frequency response of the op amp is considered to be constant. In other words, the ideal op amp is considered to have infinite bandwidth. If we assume a finite gain for the op amp, then Figure 3.2 shows the ideal op amp frequency response.

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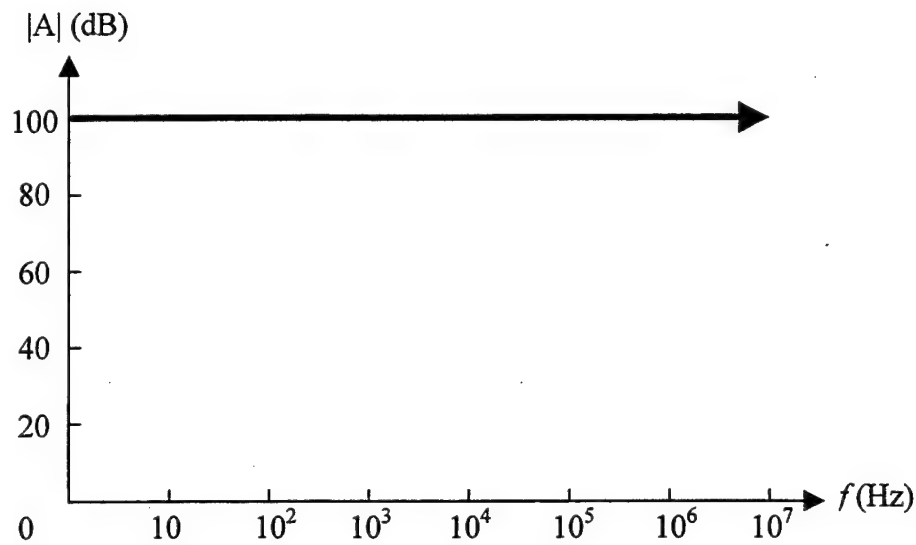
Figure 3.2: Ideal Op Amp Frequency Response

In reality, however, the op amp frequency response is not constant, rather the real op amp has a finite bandwidth. Internal circuit characteristics, such as parasitic capacitances, dictate the op amp finite bandwidth. However, in order to cause the op amp to have a single-time-constant low-pass frequency response, circuit designers normally include a compensating capacitor in the op amp design. This compensating capacitor ensures stable operation by causing the gain response to be less than one prior to the phase response reaching −180 degrees. This guarantees that negative feedback does not become positive feedback due to the phase response. Such op amps are termed *internally compensated*, and display a uniform gain rolloff, typically −20dB/decade. Figure 3.3 illustrates the non-ideal frequency response of general purpose op amps such as the 741-types. Obviously, in this parameter the real world op amp differs considerably from the ideal case. The finite bandwidth of op amps often is the limiting factor in determining the maximum operating frequency of circuits.
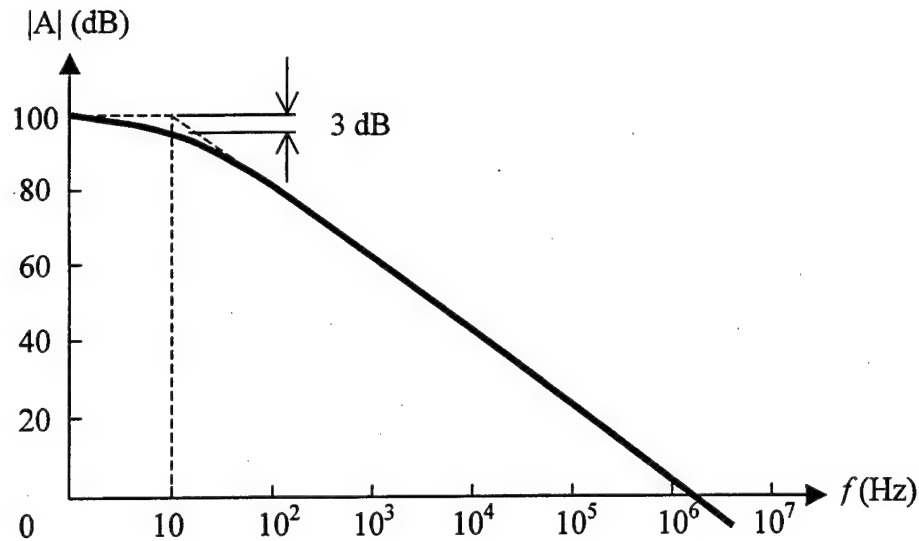
Figure 3.3: Typical Non-Ideal Op Amp Frequency Response

3.   Input Impedance

The input impedance of the op amp is defined as the ratio of the input voltage to input current. In the ideal case the op amp is considered to have infinite input impedance. That is, neither input terminal of the op amp draws any current. In the non-ideal case the input impedance of an op amp is determined by the internal circuitry used, specifically what type of transistors are used. Input impedance for the 741 op amp ranges from 100kΩ to 2MΩ. These values are typical for op amps constructed using bipolar junction transistors. Op amps constructed using MOS transistors exhibit essentially infinite input impedance due to the nature of the MOS transistor.

4.   Output Impedance

The output impedance of the op amp is defined as the ratio of open-circuit output voltage to the short-circuit output current. The ideal op amp is assumed to have zero output impedance. That is, the output voltage is assumed to be independent of the current drawn from the output. In the non-ideal case the type of transistors used to construct the op amp once again are the determining factor. Op amps constructed using bipolar

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junction transistors exhibit output impedance in the range of 40 to 100Ω, while those constructed of MOS transistors are in the range of 100Ω to 5kΩ.

5.   Finite Linear Range

Equation 3.1 shows the linear relationship between the op amp inputs and output. The equation makes no mention of an acceptable range of values for these voltages. In reality the non-ideal op amp will only exhibit this linear relation for a finite range of voltages. In general this range will be equal to a value slightly below the value of the op amp power supply. If the op amp is powered with +/-15 volts, then typical values for the linear range will be approximately +/- 12 volts.

6.   Common Mode Rejection Ratio

A common mode signal is a signal which is applied simultaneously to both inputs of the op amp. Figure 3.4 shows an op amp with an applied common mode signal.
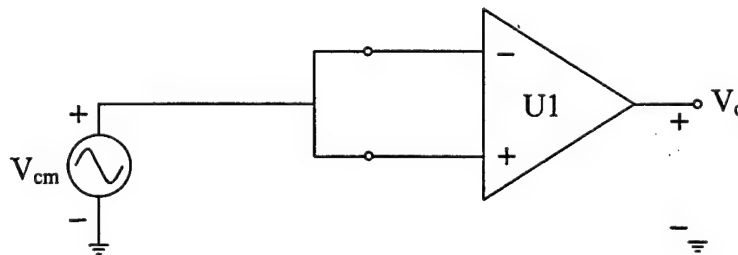
Figure 3.4: Op Amp with Common Mode Signal

Ideally the op amp will not respond to common mode signals. In other words the op amp should reject common mode signals, and only respond to differential input signals. The non-ideal op amp does show some response to common mode signals. If we let A be the differential open-loop gain of the op amp, and A_{cm} be the ratio of V_o/V_{cm} then we can define the *Common Mode Rejection Ratio (CMRR)* as

$$CMRR = \left| \frac{A}{A_{cm}} \right| \qquad \text{(Eq. 3.2)}$$

Normally the CMRR is expressed in dB:

$$CMRR = 20 \log \left| \frac{A}{A_{cm}} \right| \qquad \text{(Eq. 3.3)}$$

In general the CMRR indicates the level to which the op amp is able to reject certain common mode signals. The most important common mode signal that one would wish to reject is noise. Thus the greater the CMRR the less susceptible to noise the op amp will be.

7.   Slew Rate

The slew rate of an op amp is another important factor which determines the bandwidth of operation. The slew rate is defined as the maximum rate of change of the output voltage with respect to time

$$SR = \left. \frac{dV_o}{dt} \right|_{max} \qquad \text{(Eq. 3.4)}$$

We can see the frequency limitation due to slew rate by examining an example. If one is given a voltage signal

$$v = \hat{V} \sin \omega t \qquad \text{(Eq. 3.5)}$$

Then the first derivative of the signal with respect to time is given by

$$\frac{dv}{dt} = \omega \hat{V} \cos \omega t \qquad \text{(Eq. 3.6)}$$

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The maximum value of the derivative is

$$\left. \frac{dv}{dt} \right|_{max} = \omega_m \hat{V} \qquad \text{(Eq. 3.7)}$$

If we then equate this value to the slew rate, and solve for maximum frequency we obtain

$$f_m = \frac{SR}{2\pi\hat{V}} \qquad \text{(Eq. 3.8)}$$

Thus we see that the slew rate, along with the maximum value of the voltage signal, imposes a fundamental limitation on frequency. Circuit designers must keep this limitation in mind when developing systems. One way in which to limit the effect of the slew rate imposed frequency constraint is to keep maximum signal voltages low. This method is appropriate as long as adequate signal to noise ratios are maintained.

Values of slew rates are normally given in units of V/μs. Typical op amps exhibit slew rates of a few V/μs, while op amps constructed of MOS transistors have slew rates of 1-20 V/μs.

C. OP AMP SELECTION

The overall filtering circuit of this project, like most analog and sampled data systems, relies heavily on the use of op amps. As such, selection of an op amp appropriate to circuit requirements was critical. Several factors influenced the selection process, including op amp complexity, types of transistors used, manufacturing process to be used for construction, and performance characteristics.

Op amps are complex circuits containing many transistors. Special purpose op amps with operating parameters optimized in some way may contain dozens of transistors

of various types. For this project the complexity of the op amp circuit was important for two reasons. First, the layout of the op amp had to be done at the individual transistor level. Circuit designers would normally have access to libraries of standard cells containing many frequently used components. Op amp layout would then simply require an appropriate selection. This project did not have access to predesigned op amp layouts. The second reason for attempting to limit op amp complexity was available chip area. The fabrication process available for this project imposed constraints on the overall chip size. More complex op amps would take up more of this valuable area. For these reasons the circuit complexity influenced the op amp selection.

The types of transistors used in the op amp, and the manufacturing process available were also considered. Bipolar junction transistors are more effective at supplying large currents, while MOS transistors have an effectively infinite input impedance. Op amps have been constructed using both types of transistors, as well as combinations of the two in order garner the benefits of each. Here the manufacturing process available entered into consideration. The MOSIS process to be used in the chip fabrication was optimized to produce MOS transistors only. There was a capability to produce bipolar junction transistors, but not in an optimized fashion. Because of these two considerations it was decided to use an op amp which was constructed of only MOS transistors.

Performance characteristics were, of course, also a consideration in the selection process. The overall filtering circuit would be influenced most by the slew rate and gain bandwidth product of the op amps used. The "standard" 741 op amp exhibits a gain bandwidth product of approximately 1 MHz, and a slew rate of approximately 1.25 V/μs.

These values would be acceptable in the design, but increases here would lead to performance benefits of the completed circuit.

Silvernagle [Ref. 9] proposed an op amp design which was composed solely of MOS transistors, and exhibited a slew rate and gain bandwidth product greater than the 741. Additional research efforts verified the design and operation of this op amp. [Ref. 6] Table 3.1 shows the characteristics of the Silvernagle op amp, along with those of the 741 for comparison.

Op Amp	Slew Rate	Gain Bandwidth Product
741	1.25 V/μs	1 MHz
Silvernagle	3.85 V/μs	2.13 MHz

Table 3.1: Op Amp Performance Characteristics

The circuit of the Silvernagle op amp, containing 13 transistors, was also relatively simple. Therefore, because of performance characteristics, transistor types used, and relative simplicity, the decision was made to use the Silvernagle op amp. Figure 3.5 shows the circuit schematic of this op amp design.
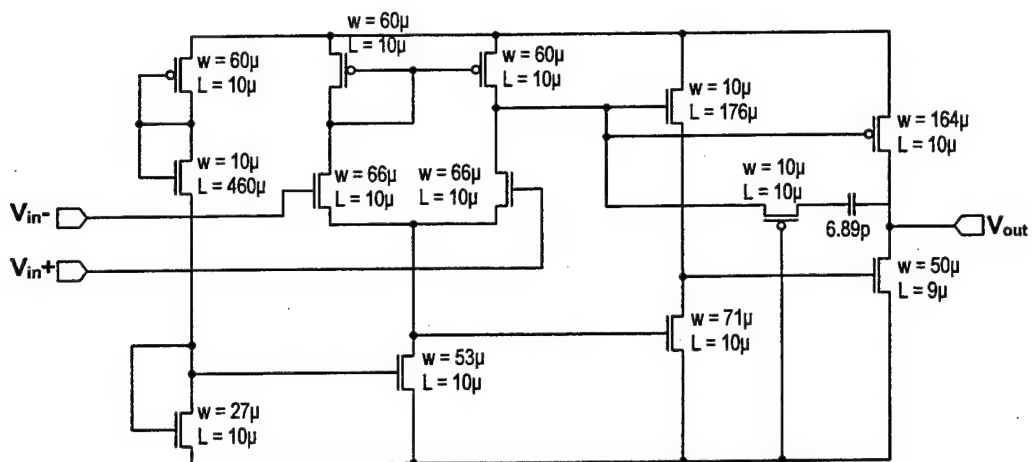
Figure 3.5: Schematic of Silvernagle Op Amp

IV.   SWITCHED CAPACITORS

A.   SWITCHED CAPACITORS VERSUS RESISTORS

Resistors are perhaps the simplest component present in any circuit network, yet their production in modern circuitry is fraught with difficulties. Modern electronics technology is centered around the use of monolithic integrated circuits (ICs). It therefore follows that integrated circuits by necessity are required to contain resistors or some type of resistance element. However, modern IC fabrication techniques can only produce resistors whose values may vary quite significantly from nominal. In fact, IC fabrication can only be counted upon to produce resistors with tolerances of 50-100% from nominal. [Ref. 2] In the context of this project resistors are needed in order to implement filtering circuits. We know that the center frequency of a filter is determined by its RC product, as shown

$$\omega_o = \frac{1}{RC} \qquad \text{(Eq. 4.1)}$$

Certainly then, if the value of R varies by 50% or more then the value of ω_0 will vary by at least that much. For effective circuit design and functioning this variation must be reduced.

These wide variations in device parameters are caused by any of a number of manufacturing process variations, including doping densities, implant doses, and variations in width and thickness of oxide layers and passive conductors. [Ref. 2] IC fabrication processes are such that these parameters will vary from day to day, and from wafer to wafer; however, the parameters are relatively consistent across any given production wafer. This in turn implies that the parameters are effectively constant across

a given integrated circuit. This consistency of parameters across a given chip will prove to be crucial in developing switched capacitor filters.

In addition to the problems associated with the tolerances of IC fabricated resistors they also suffer from additional drawbacks. IC fabrication techniques are optimized to produce transistors. In this role the fabrication techniques can efficiently produce very small transistors. When used to produce resistors, however, these same techniques are not as efficient. In fact a simple resistor on an IC will take up much more surface area than a transistor produced using the same technology family. This becomes a crucial problem, because in the electronics industry the "chip area" often dictates the cost of the entire circuit. Thus, IC fabricated resistors, in addition to having poor tolerances, are also expensive to implement.

It is possible to produce accurate resistors on integrated circuits. However, this usually requires additional steps in the manufacturing process. Laser trimming is one such technique. In laser trimming a high-powered laser vaporizes areas of the resistor until it meets a required value. This technique is, in effect, manufacturing custom chips, and hence is very time consuming and very costly.

It would seem then that the production of resistors on integrated circuits is prohibitively expensive, and laced with problems. This would imply that resistors should be avoided at all costs when designing circuits which will be produced in IC form. This however would be virtually impossible. We must then look for more accurate and cost effective ways in which to implement the function of a resistor. The switched capacitor provides us with just such a solution.

B.   INTRODUCTION TO SWITCHED CAPACITORS

A switched capacitor is a circuit topology, containing a capacitance and switches, which can be made to function as an equivalent resistance. The switched capacitor is based on the realization that a capacitor which is switched between two circuit nodes at a sufficiently high rate is equivalent to a resistor connecting these two nodes. [Ref. 3] Figure 4.1 illustrates a switched capacitor in its most basic form
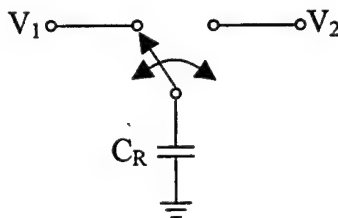

Figure 4.1: Simple Switched Capacitor Network

When the switch is connected to V_1 the capacitor will charge to that voltage, then when it connects to V_2 the capacitor will charge, or discharge, to that voltage. Thus, charge will be shuttled from one node to the other at a rate based on the switching frequency. The concept of a switched capacitor does not, on its own, provided us with a solution to fabricating accurate values of resistance unless one looks again at the manufacturing process. It turns out that modern CMOS fabrication techniques can produce capacitors whose values have much better variation from nominal than resistors. This alone provides us with some benefit; however, a tremendous additional benefit, and very close tolerances can be achieved by designing a circuit which is dependent upon a ratio of capacitances. The next section will provide more detailed explanations of switched capacitors, their implementation, and benefits.

C.   DEVELOPMENT OF SWITCHED CAPACITORS

1.   Equivalent Resistance

This section will develop the equations governing the functioning of simple switched capacitors and their equivalent resistances. Figure 4.2 illustrates a slightly more detailed switched capacitor network.
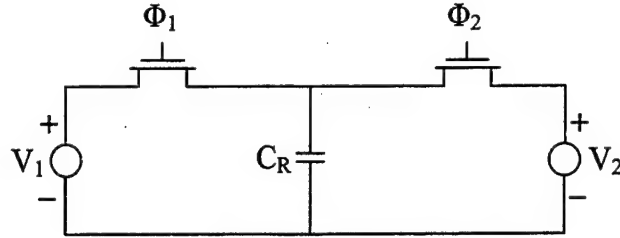

Figure 4.2: MOS Implementation of a Switched Capacitor

In this figure a pair of MOS transistors used as pass gates (switches) have replaced the simple switch shown in Figure 4.1. The inputs of the MOS transistors (Φ_1 and Φ_2) control the switching of the circuit, and represent inputs from a two-phase non-overlapping clock signal. These inputs are mutually exclusive; that is, only one is asserted at any given time. The non-overlapping clock ensures that when Φ_1 is asserted, Φ_2 is not asserted. Before Φ_2 is asserted Φ_1 is de-asserted, and so on. This non-overlapping action is required for the circuit to function correctly.

Switched capacitors operate on the principle that capacitors store a charge Q. If Φ_1 is asserted (and Φ_2 de-asserted) then the capacitor C_R will be connected to V_1. The charge stored by the capacitor is given by

$$Q_1 = C_R V_1 \qquad\qquad\qquad \text{(Eq. 4.2)}$$

Now, when Φ_2 is asserted (and Φ_1 de-asserted) C_R will become charged to V_2. However, this time the only charge flowing in the circuit is

$$Q_2 = C_R V_2 - C_R V_1 = C_R(V_2 - V_1) \qquad\qquad \text{(Eq. 4.3)}$$

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which is the difference between the charge placed on C_R by V_2 and the previous charge that was placed on C_R by V_1. [Ref. 4] When the transistors (switches) are again alternated the charge flow is

$$Q_3 = C_R V_1 - C_R V_2 = C_R(V_1 - V_2) \qquad \text{(Eq. 4.4)}$$

This sequence of events will continue for as long as the circuit is appropriately switched. Let us assume that the network is switched at a rate

$$f_c = \frac{1}{T_c} \qquad \text{(Eq. 4.5)}$$

Then the average rate of transfer of charge Q over the period T_c can be considered current flow, and can be expressed as

$$I \cong \frac{\Delta Q}{T_c} = \Delta Q f_c = f_c C_R (V_1 - V_2) \qquad \text{(Eq. 4.6)}$$

Dividing the difference in potential by I gives us the expression for resistance

$$R \cong \frac{V_1 - V_2}{I} = \frac{1}{f_c C_R} \qquad \text{(Eq. 4.7)}$$

Equation 4.7 defines the equivalent resistance of a switched capacitor network.

2.   Switched Capacitors in Filters
The advantage of utilizing switched capacitors as resistors can be appreciated by comparing the RC product of a resistor R_1 and a capacitor C_2. [Ref. 4] Let the product of R_1 and C_2 form the time constant τ, given as

$$\tau = R_1 C_2 \qquad \text{(Eq. 4.8)}$$

Equation 4.1 shows us that this time constant is the determining factor in the filter center frequency. Thus it is important to control τ as accurately as possible. The

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dependence of the accuracy of τ upon R_1 and C_2 can be found by the following expression

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \qquad \text{(Eq. 4.9)}$$

"The worst-case accuracy of τ will be the sum of the absolute accuracies of R_1 and C_2, which is very poor if R_1 and C_2 are implemented on an integrated circuit." [Ref. 4] Now let us replace R_1 with a switched capacitor equivalent. The equation for τ becomes

$$\tau = \frac{1}{f_c} \frac{C}{C_R} = T_c \frac{C}{C_R} \qquad \text{(Eq. 4.10)}$$

The accuracy of τ can then be expressed as

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_R}{C_R} \qquad \text{(Eq. 4.11)}$$

We may safely assume that T_c is perfectly accurate, which gives

$$\frac{d\tau}{\tau} = \frac{dC_2}{C_2} - \frac{dC_R}{C_R} \qquad \text{(Eq. 4.12)}$$

We may also express the center frequency of a filter realized using switched capacitors as

$$\omega_0 = \frac{C_R}{C} f_c \qquad \text{(Eq. 4.13)}$$

When constructed on an IC the two capacitances will fairly accurate. However, the ratio of the capacitances will by very accurate. Typical tolerances for this ratio are in the neighborhood of 0.1% or less.

There are several reasons for this tremendous increase in accuracy. As stated earlier the parameters of IC fabricated components (resistance per square, capacitance per unit area, etc.) are not especially accurate in the absolute sense. These parameters vary from day to day, and wafer to wafer. However, the parameters across an individual wafer, and thus across each chip, are relatively constant. Therefore, if consistent size components can be made on the same chip, then their values relative to one another will be highly accurate. Fortunately the IC fabrication process, and associated photo-lithography, are extremely adept at the layout of consistent size objects. Thus, since we have now developed a circuit topology in which the accuracy of the filter center frequency is dependent upon a *ratio* of on-chip capacitors, we have the means to develop ICs which maintain very tight tolerances in the area of interest.

D.   SAMPLED DATA SYSTEMS

1.   Transformations

In order to further develop the concepts of switched capacitor systems one must step back and examine some of the basic underlying operating principles. An *analog signal* is a signal which is continuous in both time and amplitude. A *digital signal* is a signal which is discrete in both time and amplitude. [Ref. 4] The operation of a switched capacitor system lies between these two definitions. Switched capacitor systems are *sampled data systems*. That is, due to the switching required for correct operation, they are discrete in time, but continuous in amplitude.

An appropriate analysis tool for sampled data systems is the *z*-transform. However, since filters are typically specified by frequency domain requirements, it is helpful to have a mathematical expression that allows us to transform rational *s*-domain

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transfer functions to rational z-domain transfer functions. In general, to be useful, such an expression should also possess two qualities:

1. Stable s-domain transfer functions map into stable z-domain transfer functions.

2. The imaginary $j\omega$-axis of the s-plane maps onto the unit circle of the z-plane.

Item 1 ensures that our transformed z-domain transfer function will be stable. Item 2 ensures that not only will they be stable but that the shape of the gain response can be preserved. [Ref. 5]

There are four transformations which have been used to synthesize switched capacitor networks. [Ref. 5] These transformations include the *Backward Difference* (BD), the *Forward Difference* (FD), *Bilinear*, and *Lossless Discrete Integrator* (LDI).

Previous work in this area [Ref. 6, 7] has shown that the bilinear transformation is the appropriate method for a circuit such as that used in this project. The equation of the bilinear transformation is

$$\frac{1}{s} = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} \qquad \text{(Eq. 4.14)}$$

or

$$s = \frac{2}{T}\frac{z-1}{z+1} \qquad \text{(Eq. 4.15)}$$

Figure 4.3 shows the s-to-z plane mapping of this transformation.
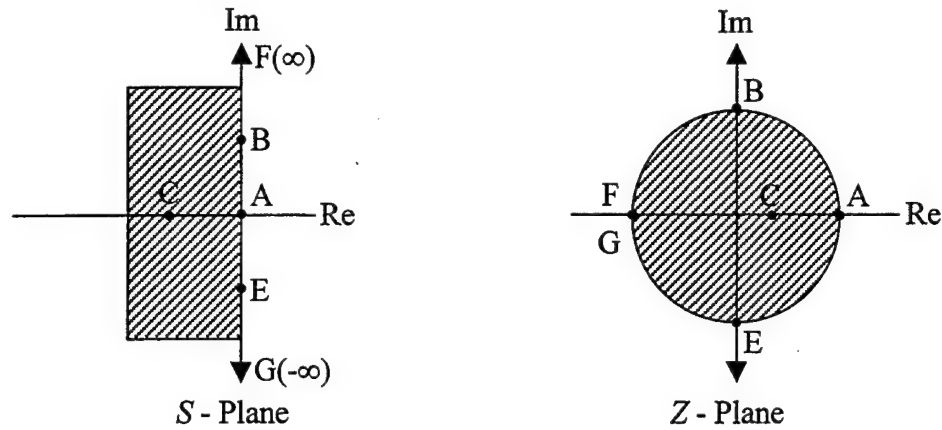
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Figure 4.3: Illustration of the Bilinear Mapping

2.   Side Effects of the Bilinear Transformation

The bilinear transformation exhibits additional properties which must be taken into account. The best known, and most important, of these properties is the frequency warping effect. This frequency warping is a direct result of the nonlinear relationship that exists between the analog frequency ω_a, where $s_a = j\omega_a$, and the sampled data domain frequency ω, where $z = e^{j\omega\gamma}$. [Ref. 5] We may illustrate the side effect by substituting $s_a = j\omega_a$ and $z = e^{j\omega\gamma}$ into Equation 4.15 and dividing both the numerator and denominator by $2e^{j\omega T/2}$

$$\frac{\omega_a T}{2} = \tan\frac{\omega T}{2}$$ (Eq. 4.16)

Then solving for ω,

$$\omega = \frac{2}{T}\tan^{-1}\left[\frac{\omega_a T}{2}\right]$$ (Eq. 4.17)

Equation 4.17 gives the difference between frequencies in the analog and sampled data domains. This warping effect comes from the transformation of a straight line in the *s*-domain into the unit circle of the *z*-domain. [Ref. 6]

There are two ways in which a designer can compensate for this effect. One method is to prewarp the cutoff and stop band edge frequencies according to Equation 4.17 [Ref. 5] Another method is to minimize the warping effect all together. The warping can be reduced to negligible levels if a clock frequency of at least ten times greater than that of the analog signal frequency is maintained. [Ref. 7] This latter method is the approach which will be used in this project.

E. THE FLOATING BILINEAR SWITCHED CAPACITOR RESISTOR

There are numerous different network topologies which can be used to implement switched capacitor resistors. [Ref. 4, 5, 7] One such topology which has proven to be successful is the *Floating Bilinear Switched Capacitor Resistor*, or simply the *Floating Bilinear Resistor (FBR)*. [Ref. 5, 6, 7] The network configuration of the FBR is shown in Figure 4.4. The goal of this section will be to develop an equation for the equivalent resistance of this network.
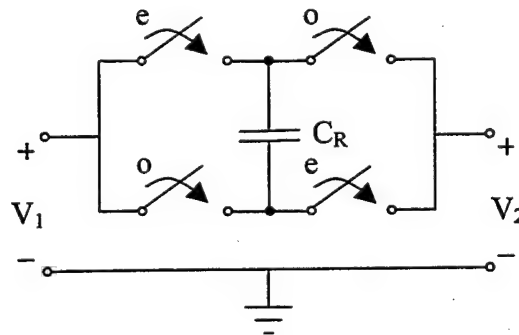

Figure 4.4: Floating Bilinear Resistor

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The 'e' in the figure denotes 'even phase' while the 'o' denotes 'odd phase'. As previously stated these phases must be non-overlapping in order for the circuit to function. If we allow the clock period to be denoted by τ, then the period $T = \tau/2$ is the time during which similar switches (the e's or the o's) are closed. Then the instantaneous charge at either node, for the even and odd sampling periods, is $\Delta q(kT)$. Then, if we write the nodal charge equations we get [Ref. 5]

For the even kT times:

$$\Delta q_1^e(kT) = Cv_1^e(kT) - Cv_1^o[(k-1)T] - Cv_2^e(kT) + Cv_2^o[(k-1)T] \qquad \text{(Eq. 4.18)}$$

$$\Delta q_2^e(kT) = Cv_2^e(kT) - Cv_2^o[(k-1)T] - Cv_1^e(kT) + Cv_1^o[(k-1)T] \qquad \text{(Eq. 4.19)}$$

For the odd kT times:

$$\Delta q_1^o(kT) = Cv_1^o(kT) - Cv_1^e[(k-1)T] - Cv_2^o(kT) + Cv_2^e[(k-1)T] \qquad \text{(Eq. 4.20)}$$

$$\Delta q_2^o(kT) = Cv_2^o(kT) - Cv_2^e[(k-1)T] - Cv_1^o(kT) + Cv_1^e[(k-1)T] \qquad \text{(Eq. 4.21)}$$

If we utilize the z-transform, where $Z[u(kT)] = U(z)$, and $Z[u[(k-1)T]] = z^{-1/2}U(z)$, then with $Q = CV$, we can obtain the z-transformed nodal charge equations for the FBR

$$\Delta Q_1^e(z) = CV_1^e(z) + Cz^{\frac{-1}{2}}V_1^o(z) - CV_2^e(z) - Cz^{\frac{-1}{2}}V_2^o(z) \qquad \text{(Eq. 4.22)}$$

$$\Delta Q_1^o(z) = CV_1^o(z) + Cz^{\frac{-1}{2}}V_1^e(z) - CV_2^o(z) - Cz^{\frac{-1}{2}}V_2^e(z) \qquad \text{(Eq. 4.23)}$$

$$\Delta Q_2^e(z) = CV_2^e(z) + Cz^{\frac{-1}{2}}V_2^o(z) - CV_1^e(z) - Cz^{\frac{-1}{2}}V_1^o(z) \qquad \text{(Eq. 4.24)}$$

$$\Delta Q_2^o(z) = CV_2^o(z) + Cz^{\frac{-1}{2}}V_2^e(z) - CV_1^o(z) - Cz^{\frac{-1}{2}}V_1^e(z) \qquad \text{(Eq. 4.25)}$$

If we add the two equations for each node, and reduce them we get

$$\Delta Q_1(z) = C\left(1 + z^{\frac{-1}{2}}\right)V_1(z) - C\left(1 + z^{\frac{-1}{2}}\right)V_2(z) \qquad \text{(Eq. 4.26)}$$

$$\Delta Q_2(z) = C\left(1 + z^{\frac{-1}{2}}\right)V_2(z) - C\left(1 + z^{\frac{-1}{2}}\right)V_1(z) \qquad \text{(Eq. 4.27)}$$

Ghausi and Laker [Ref. 5] demonstrate to us that when we are writing nodal charge equations we will naturally come across admittances which are not of the usual *I-V* form, but rather of the form $y = \Delta Q/V$. We may demonstrate this by looking at the equation for instantaneous voltage and current in a resistor, $i = Gv$, then substitute in the discrete time charge relation, and take the z-transform. The resulting z-domain admittance for a resistor is

$$y_R = \frac{\Delta Q(z)}{V(z)} \qquad \text{(Eq. 4.28)}$$

Using the relation of Equation 4.28 we my restate Equations 4.26 and 4.27 as

$$\Delta Q_1(z) = y_R(z)V_1(z) - y_R(z)V_2(z) \qquad \text{(Eq. 4.29)}$$

$$\Delta Q_2(z) = y_R(z)V_2(z) - y_R(z)V_1(z) \qquad \text{(Eq. 4.30)}$$

Thus, with $z = e^{s\tau}$, we can say

$$y_R = C\left(1 + z^{\frac{-1}{2}}\right) \qquad \text{(Eq. 4.31)}$$

or with $\hat{z} = e^{\frac{s\tau}{2}}$

$$y_R = C\left(1 + \hat{z}^{-1}\right) \qquad \text{(Eq. 4.32)}$$

Equations 4.31 and 4.32 are the equations for the equivalent admittance of a floating bilinear resistor. However, we desire to develop equations which are not dependent on z.

We may accomplish this by generating another equation for the z-domain admittance of a resistor, and equating it to Equation 4.31 or 4.32. We may generate such an equation by first looking at the Laplace domain admittance of a resistor, then using the equation of the bilinear transformation (Equation 4.15) to change it into the z-domain. [Ref. 5] Table 4.1 illustrates the Laplace domain admittances of circuit components, and the equivalent admittance transformed to the z-domain by the bilinear transformation.

	Circuit Element		
	Capacitor	Resistor	Inductor
Laplace Domain Admittance	sC	G	$1/sL$
Z-Domain Admittance after Bilinear Transform	$C(1-z^{-1})$	$\dfrac{G\tau}{2}(1+z^{-1})$	$\dfrac{\tau^2}{4L}\dfrac{(1+z^{-1})^2}{1-z^{-1}}$

Table 4.1: Equivalent Admittances

Then, if we set the equivalent admittance of Equation 4.32 equal to that of table 4.1, we have, for a half clock cycle

$$C(1+z^{-1}) = \frac{G\tau(1+z^{-1})}{2} \qquad \text{(Eq. 4.33)}$$

We can then solve Equation 4.33 for G, to get

$$G = \frac{2C}{\tau} \qquad \text{(Eq. 4.34)}$$

Similarly, by using Equation 4.31 we may obtain the equivalent admittance for a full clock cycle

$$G = \frac{4C}{\tau} \qquad \text{(Eq. 4.35)}$$

Thus we have developed the desired equations for the equivalent resistance of the floating bilinear resistor. Using these equations one may chose appropriate value capacitors and clocking speeds to implement the desired resistance values. This is the technique which will be used in the development of the overall filter design of this project.

F. TWO PHASE NON-OVERLAPPING CLOCK

A crucial portion of any switched capacitor network is the two phase non-overlapping clock circuit. It is this clocking circuit which provides the "switching" of the "switched" capacitor. Without the proper clocking a switched capacitor network will not function properly, or could provide a direct, short circuit path between two voltage nodes. Figure 4.5 illustrates the output of such a clocking circuit.
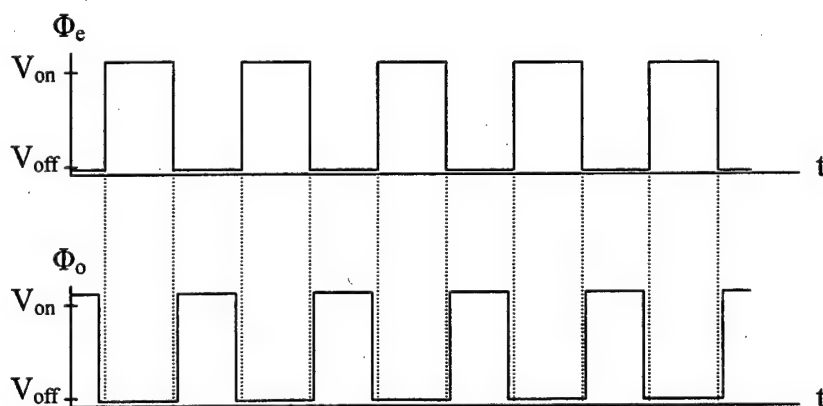
Figure 4.5: Two Phase Non-Overlapping Clock Output

The circuitry for the two phase clock is based on a cross-coupled RS flip-flop, and is relatively simple. [Ref. 2] Previous work in the area of switched capacitor filters has shown that the structure of Figure 4.6 is an appropriate one to use. [Ref. 6]
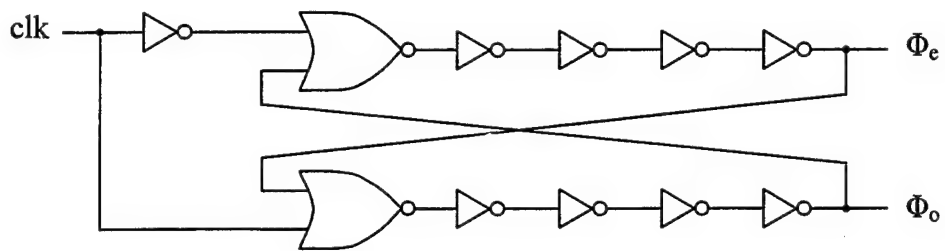
Figure 4.6: Two Phase Non-Overlapping Clock Circuit

This is the circuit structure that will be used for the required clocking in this project.

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V.   THE GIC FILTER

A.   BACKGROUND

It has been shown that in order to implement all possible filter types using passive components a circuit network must contain resistors, capacitors, and inductors. Modern IC manufacturing techniques allow for the accurate construction of capacitors, and Chapter 4 demonstrated a method for the elimination of resistors by using switched capacitors. However, we are still left with the problem of inductors. Discrete inductors of suitable impedance values are available for use in circuits. However, these inductors tend to be large and costly. Additionally, the focus of modern electronics is on fully integrated circuits. Integrated circuit manufacture of suitable inductors is very difficult, if not impossible. IC inductors take up vast quantities of valuable chip area, and suffer from terrible tolerances. How then can we develop the full range of filter types in light of the problems involving inductors?

It was recognized in the 1950s that size and cost reductions, along with performance increases, could be achieved by replacing the large costly inductors used in circuits with active networks. [Ref. 6] This is not to say that the need for an inductive impedance was obviated. Rather, a suitable replacement, or means of simulation was necessary. A variety of methods for the simulation of inductances have been developed. One of the most important and useful of these methods is the *Generalized Immittance Converter* (GIC) developed by Antoniou et al. [Ref. 10] This circuit is also sometimes referred to as the *Generalized Impedance Converter*. One of the most important applications of the GIC is inductor simulation. [Ref. 6] The next section will show how

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this circuit network containing op amps, resistors, and capacitors can effectively simulate accurate inductance values.

B.   INDUCTOR SIMULATION

In order to demonstrate how a GIC can be used to simulate inductors we will examine the basic GIC circuit. This circuit will be specified with generic impedance values (Z_i). Network analysis will be used to determine the input impedance of the circuit. Once an equation for the input impedance, in terms of generic impedance values, is found, then specifications of the impedances required for inductor simulation can be made. The circuit network of the GIC with generic impedances is shown in Figure 5.1.
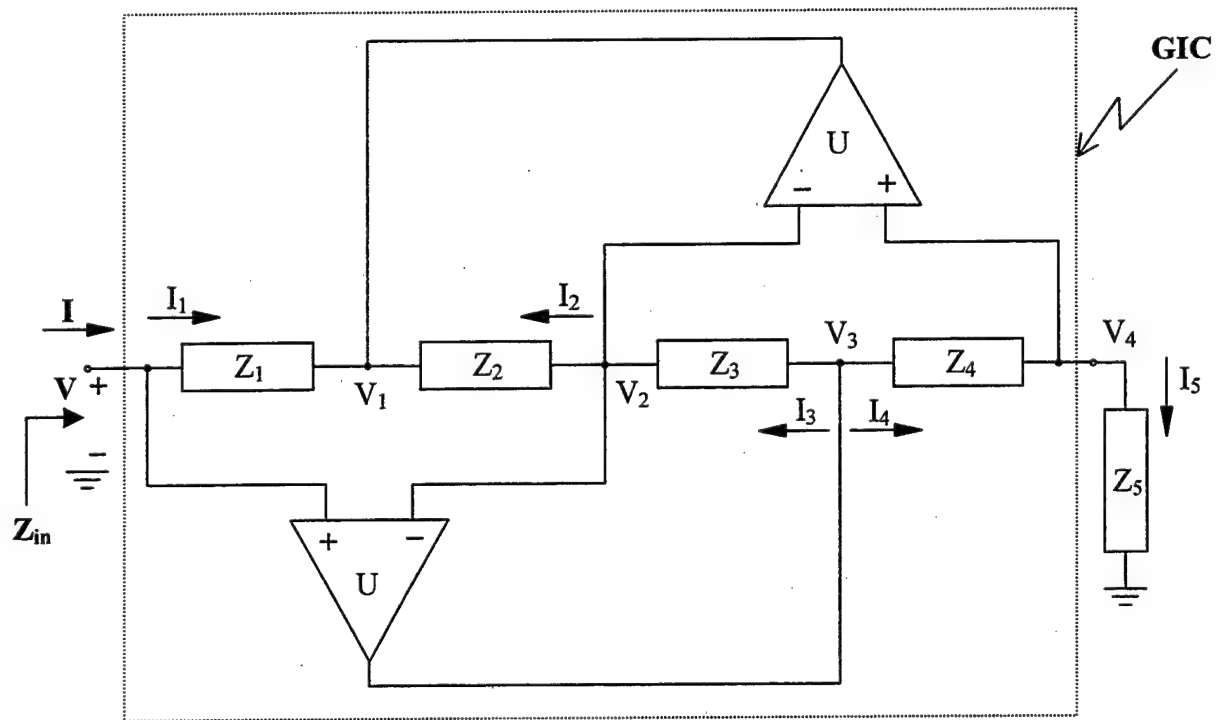
Figure 5.1: GIC Network for Inductor Simulation

We can then begin the nodal analysis of the circuit. We know that the input impedance is given by

$$Z_{in} = \frac{V}{I}$$

(Eq. 5.1)

The current at the load impedance is

$$I_5 = \frac{V_4}{Z_5} = \frac{V}{Z_5}$$

(Eq. 5.2)

Where the second equality stems from the virtual short circuit that exists from the input voltage to V_4 across the input terminals of the two op amps. Then, if we note that the input impedance of the op amps is theoretically infinite, that is, they draw no current, we can see

$$I_4 = I_5 = \frac{V}{Z_5}$$

(Eq. 5.3)

Then examining the voltage at V_3 we find

$$V_3 = V_4 + I_4 Z_4$$

(Eq. 5.4)

Next we can substitute in the value of I_4 from Equation 5.3, and the relation $V_4 = V$ due to the virtual short circuit, to yield

$$V_3 = \left(1 + \frac{Z_4}{Z_5}\right)V$$

(Eq. 5.5)

Then if we examine the current I_3 we find

$$I_3 = \frac{V_3 - V_2}{Z_3} = \frac{\left[\left(1 + \dfrac{Z_4}{Z_5}\right)V - V\right]}{Z_3}$$

(Eq. 5.6)

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Where the second equality results from the same substitutions used to generate Equation 5.5. We may simplify Equation 5.6 to the following

$$I_3 = \frac{Z_4}{Z_5}\frac{V}{Z_3} \qquad \text{(Eq. 5.7)}$$

Here we can note that if we sum the currents at V_2, and assume that the op amps draw no, or negligible, current then

$$I_2 = I_3 \qquad \text{(Eq. 5.8)}$$

Next, the voltage at V_1 is found to be

$$V_1 = V_2 - I_2 Z_2 = V - I_3 Z_2 = V - V\frac{Z_4 Z_2}{Z_5 Z_3} \qquad \text{(Eq. 5.9)}$$

The current I_1 is given by

$$I_1 = \frac{V - V_1}{Z_1} = \frac{V - V + V\left(\dfrac{Z_2 Z_4}{Z_3 Z_5}\right)}{Z_1} = V\left(\frac{Z_2 Z_4}{Z_1 Z_3 Z_5}\right) \qquad \text{(Eq. 5.10)}$$

Here if we note that obviously $I = I_1$, then we can write the equation for the input impedance of the circuit as

$$Z_{in} \equiv \frac{V}{I} = \frac{Z_1 Z_3}{Z_2 Z_4} Z_5 \qquad \text{(Eq. 5.11)}$$

Thus we have the input impedance of the GIC in terms of generic impedances. Next we must chose these impedances so that the circuit functions as we desire, that is, it simulates an inductance. If we choose the components as follows

$$Z_1 = R_1, \quad Z_3 = R_3, \quad Z_4 = R_4, \quad Z_5 = R_5$$
$$\text{and } Z_2 = \frac{1}{sC}$$

Then substitution of these components into Equation 5.11 yields

$$Z_{in} = sC\frac{R_1 R_3 R_5}{R_4} \qquad \text{(Eq. 5.12)}$$

or

$$Z_{in} = sL, \quad \text{where } L = C\frac{R_1 R_3 R_5}{R_4} \qquad \text{(Eq. 5.13)}$$

In others words the capacitor of the circuit will act as an inductor with an inductance determined by the value of the capacitor and the resistances used. This is an extremely important result. We have shown that the GIC can be used to effectively simulate inductances. Thus we have the means to eliminate another circuit component which is difficult and costly to fabricate using modern integrated circuit technology.

The next section will extend the concept of the GIC one step further. Using a slightly more general circuit arrangement we can develop the GIC Filter. The circuit network of the GIC Filter will be able to provide all of the basic filter types when the components are selected correctly.

C.   GIC FILTER

The previous section demonstrated the use of the GIC for inductor simulation. This result is noteworthy and useful; however, the GIC has even greater application when used as a filter. A GIC filter network is capable of performing all of the basic filtering types, with a minimum of component variation. That is, the GIC filter network arrangement remains the same regardless of the filter type. The only change necessary to implement a different filter type is a change of a few components.

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For the development here it is more convenient to work with admittance values, vice the impedances previously used. We will also continue the assumption that the op amps used are ideal (i.e. exhibit an infinite bandwidth and infinite input impedance). Figure 5.2 shows the circuit network of the GIC filter with generic admittance values.
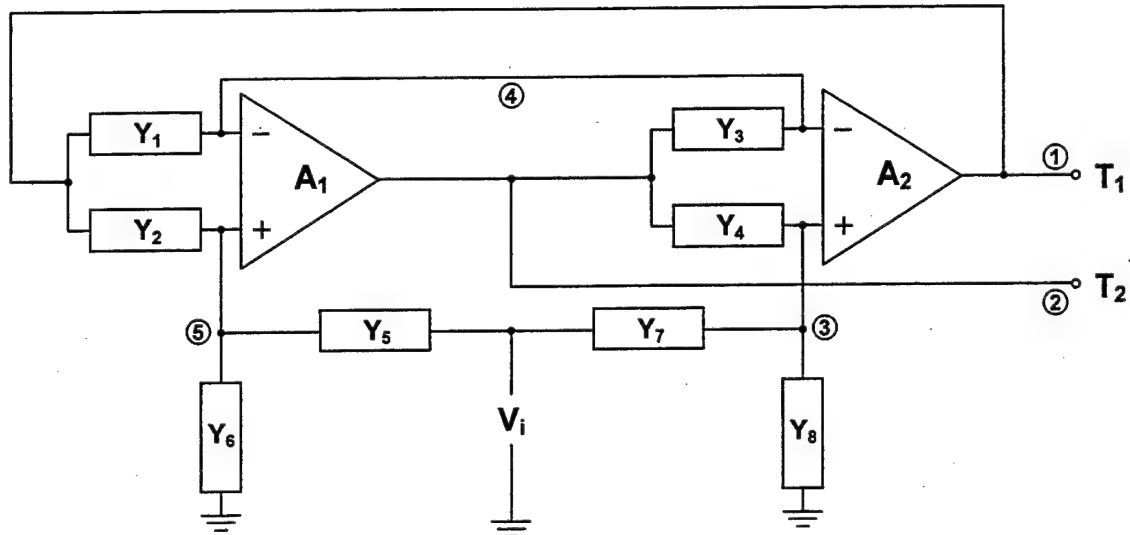
Figure 5.2: The GIC Filter Circuit Network

The first goal will be to develop the transfer function of the circuit in terms of the generic admittance values. Then we can substitute in values for the admittances in order to realize the various filter types. Note that two output nodes are specified in the circuit. These are necessary for realization of the four filter types. Transfer functions for each node will be developed.

The first step in deriving the transfer function is to count the circuit nodes, and find an appropriate number of equations for those nodes (one equation fewer than the number of nodes). At first glance the circuit appears to have six nodes (V_i, and nodes 1-5). However, because of the virtual short circuit across the inputs of an ideal op amp,

nodes 3, 4, and 5 are at the same potential. Therefore, the circuit actually has only four nodes. For clarity in specifying the location at which equations are derived we will continue using the notation of the six nodes shown, but make the substitutions $V_4 = V_5 = V_3$ whenever necessary. With only four nodes we only require three equations for the circuit. If we sum the currents at the node labeled 5 we have

$$(V_i - V_3)Y_5 = (V_3 - 0)Y_6 + (V_3 - V_1)Y_2 \quad \Rightarrow \quad V_iY_5 - V_3Y_5 = V_3Y_6 + V_3Y_2 - V_1Y_2 \qquad \text{(Eq. 5.14)}$$

Then if we sum the currents at the node labeled 3 we get

$$(V_i - V_3)Y_7 = (V_3 - 0)Y_8 + (V_3 - V_2)Y_4 \quad \Rightarrow \quad V_iY_7 - V_3Y_7 = V_3Y_8 + V_3Y_4 - V_2Y_4 \qquad \text{(Eq. 5.15)}$$

We can obtain our final necessary equation by summing current at node 4, with the assumption that the op amps have infinite input impedance (i.e. the op amps draw no current).

$$(V_1 - V_3)Y_1 = (V_3 - V_2)Y_3 \quad \Rightarrow \quad V_1Y_1 - V_3Y_1 = V_3Y_3 - V_2Y_3 \qquad \text{(Eq. 5.16)}$$

Equations 5.14, 5.15, and 5.16 can be used to determine the transfer function of the circuit. If we first solve Equation 5.14 for V_3 we obtain

$$V_3 = \frac{V_iY_5 + V_1Y_2}{(Y_2 + Y_5 + Y_6)} \qquad \text{(Eq. 5.17)}$$

Next, solving Equation 5.15 for V_2 yields

$$V_2 = V_3\frac{Y_4}{Y_4} + V_3\frac{Y_7}{Y_4} + V_3\frac{Y_8}{Y_4} - V_i\frac{Y_7}{Y_4} \qquad \text{(Eq. 5.18)}$$

Now if we substitute Equation 5.17 into Equation 5.18 we find

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$$V_2 = \frac{V_iY_4Y_5 + V_1Y_2Y_4 + V_iY_5Y_7 + V_1Y_2Y_7 + V_iY_5Y_8 + V_1Y_2Y_8 - V_iY_2Y_7 - V_iY_5Y_7 - V_iY_6Y_7}{Y_4(Y_2 + Y_5 + Y_6)}$$

<div align="center">or</div>
(Eq. 5.19)

$$V_2 = \frac{V_1(Y_2Y_4 + Y_2Y_7 + Y_2Y_8) + V_i(Y_4Y_5 + Y_5Y_8 - Y_2Y_7 - Y_6Y_7)}{Y_2Y_4 + Y_4Y_5 + Y_4Y_6}$$

If we then substitute Equations 5.17 and 5.19 into Equation 5.16 we have

$$V_1Y_1 - \left[\frac{V_iY_1Y_5 + V_1Y_1Y_2}{Y_2 + Y_5 + Y_6}\right] = \left[\frac{V_iY_3Y_5 + V_1Y_2Y_3}{Y_2 + Y_5 + Y_6}\right] - \left[\begin{array}{c}\dfrac{V_1(Y_2Y_3Y_4 + Y_2Y_3Y_7 + Y_2Y_3Y_8)}{Y_2Y_4 + Y_4Y_5 + Y_4Y_6} + \cdots \\[2mm] \cdots \dfrac{V_i(Y_3Y_4Y_5 + Y_3Y_5Y_8 - Y_2Y_3Y_7 - Y_3Y_6Y_7)}{Y_2Y_4 + Y_4Y_5 + Y_4Y}\end{array}\right]$$
(Eq. 5.20)

Finally, rearranging Equation 5.20 yields the transfer function of the circuit for output taken at T_1.

$$T_1 = \frac{V_1}{V_i} = \frac{Y_1Y_4Y_5 + Y_2Y_3Y_7 + Y_3Y_6Y_7 - Y_3Y_5Y_8}{Y_1Y_4Y_5 + Y_1Y_4Y_6 + Y_2Y_3Y_7 + Y_2Y_3Y_8}$$

<div align="center">or</div>
(Eq. 5.21)

$$T_1 = \frac{V_1}{V_i} = \frac{Y_1Y_4Y_5 + Y_3Y_7(Y_2 + Y_6) - Y_3Y_5Y_8}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)}$$

The transfer function for output taken at T_2 can be found using the same procedure.

$$T_2 = \frac{V_2}{V_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4Y_5 + Y_1Y_4Y_6 + Y_2Y_3Y_7 + Y_2Y_3Y_8}$$

<div align="center">or</div>
(Eq. 5.22)

$$T_2 = \frac{V_2}{V_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)}$$

Now that we have the transfer functions of the circuit we may substitute in values of the admittances in order to realize the various filter types. For example, if one wishes to realize a high pass filter the following admittance values could be used.

$$Y_1 = G \quad Y_2 = G \quad Y_3 = sC \quad Y_4 = G$$
$$Y_5 = 0 \quad Y_6 = G \quad Y_7 = sC \quad Y_8 = G$$

Entering these values into Equation 5.21 yields

$$T_1 = \frac{(GG0) + (sCsC)(G+G) - (sCG0)}{(GG)(0+G) + GsC(sC+G)} = \frac{2GC^2 s^2}{G^3 + GC^2 s^2 + G^2 Cs}$$

(Eq. 5.23)

$$\therefore T_1 = \frac{2s^2}{s^2 + \dfrac{G}{C}s + \dfrac{G^2}{C^2}} = \frac{2s^2}{s^2 + \dfrac{1}{RC} + \dfrac{1}{R^2 C^2}}$$

The last equality of Equation 5.23 is the form of a high pass filtering function with $\omega_p = 1/RC$. As previous stated, the GIC filter network can realize all of the basic filter types with only a few component variations. Table 5.1 shows the admittances required for each of the various filters, and a specification as to which output must be used. Once again, the filter cutoff (or center) frequency is given by $\omega_p = 1/RC$, while the quality factor is given by Q_p.

Examination of the table will reveal several noteworthy characteristics of this filter. First, all the resistance values used can be the same, except for one. The one different resistance is the sole item which determines the quality factor. Thus, setting or modifying the quality factor of the circuit is a straightforward procedure. Second, the admittance values of the various filter types are similar. That is, to realize one filter type

vice another requires only a small change in the network. For example, a band-pass filter and a high-pass filter use the same components, with the simple change of Y_7 and Y_8 switched. Third, zeros appear several times in the table. Since we are dealing with admittance values vice impedances the zeros indicate an open circuit. That is, a zero in the table indicates we may simply remove that component from the network, and not replace the component with anything at all.

Filter Type	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Transfer Function
Low-Pass	G	sC	$sC + \dfrac{G}{Q_p}$	G	G	0	0	G	$T_2 = \dfrac{2\omega_p^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
High-Pass	G	$\dot{G}$	sC	G	0	G	sC	$\dfrac{G}{Q_p}$	$T_1 = \dfrac{2s^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Band-Pass	G	G	sC	G	0	G	$\dfrac{G}{Q_p}$	sC	$T_1 = \dfrac{2\dfrac{\omega_p}{Q_p}s}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Notch	G	G	sC	G	G	0	sC	$\dfrac{G}{Q_p}$	$T_2 = \dfrac{s^2 + \omega_p^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$

Table 5.1: Admittance Values for GIC Filter

Thus we have determined the transfer functions of the GIC filter network, and demonstrated how this network can be used to realize all of the basic filter types. Up until this point we have used the assumption of ideal op amps. This assumption is valid for basic development, and indeed, the idealized transfer functions may be used when designing a simple GIC filter. However, part of the goal of this project is the design and implementation of high accuracy filters. To achieve the desired accuracy we can not treat the op amps as ideal. Therefore, the next section will develop the transfer function of the GIC filter with non-ideal op amps. This result will also be used later to develop the z-domain non-ideal transfer function of the network.

D.   GIC FILTER NON-IDEAL TRANSFER FUNCTION

Development of the non-ideal transfer functions requires the addition of a non-ideal model for the op amps. The main ideal characteristic we have used to this point is the assumption that the op amps had an infinite bandwidth. Now we must assume a finite bandwidth. A first order model for the op amp finite bandwidth will be used. One could use a higher order model for the op amp, but the additional orders do not provide a significant difference in results. Therefore, a first order model is suitable. Equation 5.24 shows the non-ideal op amp model, where the gain is A, while the unity-gain bandwidth is denoted ω_t.

$$A = \frac{\omega_t}{s}$$ (Eq. 5.24)

The inclusion of this non-ideal op amp model means that the GIC filter circuit can no longer be treated as having only four nodes. Rather, the circuit must be examined

using the six nodes previously mentioned and shown in Figure 5.2 (V_i plus the five numbered nodes.

Since we have six circuit nodes we require five equations in order to determine the transfer function. Those five equations are shown below as Equations 5.25 to 5.29.

$$V_2 = A_1(V_5 - V_4) \qquad\qquad \text{(Eq. 5.25)}$$

$$V_1 = A_2(V_3 - V_4) \qquad\qquad \text{(Eq. 5.26)}$$

$$V_5(Y_2 + Y_5 + Y_6) = V_1 Y_2 + V_i Y_5 \qquad\qquad \text{(Eq. 5.27)}$$

$$V_3(Y_4 + Y_7 + Y_8) = V_2 Y_4 + V_i Y_7 \qquad\qquad \text{(Eq. 5.28)}$$

$$V_4(Y_1 + Y_3) = V_1 Y_1 + V_2 Y_3 \qquad\qquad \text{(Eq. 5.29)}$$

Here, in order to simplify the calculations, I will make three substitutions. Once the transfer functions have been developed in terms of the substitution variables and generic admittance values then we may re-substitute in the values of the variables.

$$B = (Y_1 + Y_3) \qquad\qquad \text{(Eq. 5.30)}$$

$$C = (Y_4 + Y_7 + Y_8) \qquad\qquad \text{(Eq. 5.31)}$$

$$D = (Y_2 + Y_5 + Y_6) \qquad\qquad \text{(Eq. 5.32)}$$

Equations 5.25 and 5.26 do not change with the substitutions, however, if we use the three substitutions in Equations 5.27 to 5.29 we have the following

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$$V_5 = \frac{V_1 Y_2 + V_i Y_5}{D}$$ (Eq. 5.33)

$$V_3 = \frac{V_2 Y_4 + V_i Y_7}{C}$$ (Eq. 5.34)

$$V_4 = \frac{V_1 Y_1 + V_2 Y_3}{B}$$ (Eq. 5.35)

Using these equations we may now begin to solve for the non-ideal transfer function. Once again we shall determine the transfer function at T_1 then state the transfer function at T_2. The derivation of the function for output at T_2 is analogous to that for T_1. We may begin by substituting Equation 5.35 into Equation 5.25, which yields

$$V_2 = A_1 V_5 - A_1 \left(\frac{V_1 Y_1 + V_2 Y_3}{B} \right)$$

$$\therefore \quad V_2 (B + A_1 Y_3) = A_1 V_5 B - A_1 V_1 Y_1$$ (Eq. 5.36)

Substitution of Equation 5.33 into 5.36 yields

$$V_2 (B + A_1 Y_3) = A_1 B \left(\frac{V_1 Y_2 + V_i Y_5}{D} \right) - A_1 V_1 Y_5$$

$$\therefore \quad V_2 (BD + A_1 Y_3 D) = V_1 (A_1 Y_2 B - A_1 Y_1 D) + A_1 V_i Y_5 B$$ (Eq. 5.37)

Substitution of Equation 5.35 into 5.26 yields

$$V_1 = A_2 V_3 - A_2 \left(\frac{V_1 Y_1 + V_2 Y_3}{B} \right)$$

$$\therefore \quad V_1 (B + A_2 Y_1) = A_2 V_3 B - A_2 V_2 Y_3$$ (Eq. 5.38)

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Substitution of Equation 5.34 into 5.38 yields

$$V_1(B + A_2 Y_1) = A_2 B\left(\frac{V_2 Y_4 + V_i Y_7}{C}\right) - A_2 V_2 Y_3$$

$$\therefore \quad V_1(BC + A_2 Y_1 C) = V_2(A_2 Y_4 B - A_2 Y_3 C) + V_i(A_2 Y_7 B) \qquad \text{(Eq. 5.39)}$$

Then if we substitute Equation 5.37 into 5.39 and algebraically manipulate the values we get

$$V_1(BC + A_2 Y_1 C) = [A_2 Y_4 B - A_2 Y_3 C]\left[\frac{V_1(A_1 Y_2 B - A_1 Y_1 D) + A_1 V_i Y_5 B}{(BD + A_1 Y_3 D)}\right] + V_i(A_2 Y_7 B)$$

$$\therefore \quad V_1[(BC + A_2 Y_1 C)(BD + A_1 Y_3 D) - (A_1 Y_2 B - A_1 Y_1 D)(A_2 Y_4 B - A_2 Y_3 C)] =$$
$$V_i[(A_1 Y_5 B)(A_2 Y_4 B - A_2 Y_3 C) + (A_2 Y_7 B)(BD + A_1 Y_3 D)]$$

$$\therefore \quad \frac{V_1}{V_i} = \frac{A_2 Y_7 BD + A_1 A_2(Y_4 Y_5 B + Y_3 Y_7 D - Y_3 Y_5 C)}{BCD + A_2 Y_1 CD + A_1 Y_3 CD + A_1 A_2(Y_2 Y_3 C + Y_1 Y_4 D - Y_2 Y_4 B)}$$

$$\therefore \quad \frac{V_1}{V_i} = \frac{\left(Y_7 BD\dfrac{1}{A_1}\right) + (Y_4 Y_5 B + Y_3 Y_7 D - Y_3 Y_5 C)}{BCD\dfrac{1}{A_1 A_2} + Y_1 CD\dfrac{1}{A_1} + Y_3 CD\dfrac{1}{A_2} + (Y_2 Y_3 C + Y_1 Y_4 D - Y_2 Y_4 B)} \qquad \text{(Eq. 5.40)}$$

Equation 5.40 represents the non-ideal transfer function at T_1 in terms of generic admittance values, the three substitution variables used (B, C, & D), and the non-ideal amplifier gain A. We must now substitute back in the values of B, C, and D, and also

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enter the first order model for the amplifier gain. The expansion of the three substitution variables results in the following.

<div style="text-align:right">(Eq. 5.41)</div>

$$\frac{V_1}{V_i}=\frac{\dfrac{Y_7(Y_1+Y_3)(Y_2+Y_5+Y_6)}{A_1}+\left[Y_4Y_5(Y_1+Y_3)+Y_3Y_7(Y_2+Y_5+Y_6)-Y_3Y_5(Y_4+Y_7+Y_8)\right]}{\dfrac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{A_1A_2}+\dfrac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{A_1}+\dfrac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{A_2}+\left[Y_2Y_3(Y_4+Y_7+Y_8)+Y_1Y_4(Y_2+Y_5+Y_6)-Y_2Y_4(Y_1+Y_3)\right]}$$

Finally, entering the first order non-ideal op amp model and simplifying yields the complete non-ideal transfer function for output taken at T_1.

<div style="text-align:right">(Eq. 5.42)</div>

$$T_1=\frac{V_1}{V_i}=\frac{\dfrac{[Y_7(Y_1+Y_3)(Y_2+Y_5+Y_6)]}{\omega_{t_1}}s+\left[Y_1Y_4Y_5+Y_2Y_3Y_7+Y_3Y_6Y_7-Y_3Y_5Y_8\right]}{\dfrac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}\omega_{t_2}}s^2+\dfrac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}}s+\dfrac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_2}}s+\left[Y_1Y_4(Y_5+Y_6)+Y_2Y_3(Y_7+Y_8)\right]}$$

By similar means the non-ideal transfer function for output taken at T_2 can be found to be

<div style="text-align:right">(Eq. 5.43)</div>

$$T_2=\frac{V_2}{V_i}=\frac{\dfrac{[Y_5(Y_1+Y_3)(Y_4+Y_7+Y_8)]}{\omega_{t_1}}s+\left[Y_1Y_4Y_5+Y_1Y_5Y_8+Y_2Y_3Y_7-Y_1Y_6Y_7\right]}{\dfrac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}\omega_{t_2}}s^2+\dfrac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}}s+\dfrac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_2}}s+\left[Y_1Y_4(Y_5+Y_6)+Y_2Y_3(Y_7+Y_8)\right]}$$

Examination of the non-ideal transfer functions shows that, indeed, for ideal op amps ($\omega_t \to \infty$) the equations simplify to those equations found in the previous section. One can also see that with the non-ideal op amps and generic admittances the transfer

functions are second order. Therefore, if we substitute in values for the admittances based on Table 5.1 the resulting filter equations will be fourth order.

We have now developed all of the relevant concepts involved with the basic GIC and GIC filter. We have seen how the GIC can be used to simulate inductances, and how the GIC filter network can be used to realize any of the basic filter types. We have also developed both the ideal and non-ideal transfer functions of the GIC filter in terms of generic admittance values. The next chapter will delve into some advanced concepts of the GIC filter. The method of implementing the GIC filter so that it is digitally programmable and suitable for IC fabrication will be shown. Additionally, the z-domain transfer function of the GIC filter will be developed.

VI.   ADVANCED GIC DEVELOPMENTS

The previous chapters have introduced and developed several basic and important topics. This chapter will integrate several of these basic topics, and develop some of the advanced concepts necessary for this project. The first section will present a method for determining the z-domain transfer function of switched-capacitor GIC filters. The second half of the chapter will be devoted to the development of the circuit which is the goal of this project – a digitally programmable GIC filter.

A.   THE Z-DOMAIN TRANSFER FUNCTION

Chapter V developed the concept of the GIC filter and showed how it could be used to realize any of the basic filter types. However, the GIC filter of Chapter V relied on discrete components, which included resistors. In order for this design to be applicable in modern IC manufacturing we must eliminate the resistors. The use of switched-capacitors will allow the manufacture of highly accurate resistance values. By using switched-capacitors we bring the operation of the filter into the sampled data realm. Thus, the z-domain transfer function becomes the appropriate way to specify the equation of the filter. The development of this transfer function will rely upon the previously developed s-domain transfer functions, and on the concept of z-domain equivalent admittances. [Ref. 6]

Chapter IV introduced switched-capacitors, and stated that the *Floating Bilinear Resistor (FBR)* was an appropriate equivalent resistance for this circuit. Figure 6.1(a) repeats the diagram of FBR, while Figure 6.1(b) shows a more convenient diagram in which the switches have been replaced by passgates. The notation inside each passgate

indicates the clock cycle in which the gate is active (i.e. the clock cycle during which the switch is closed).
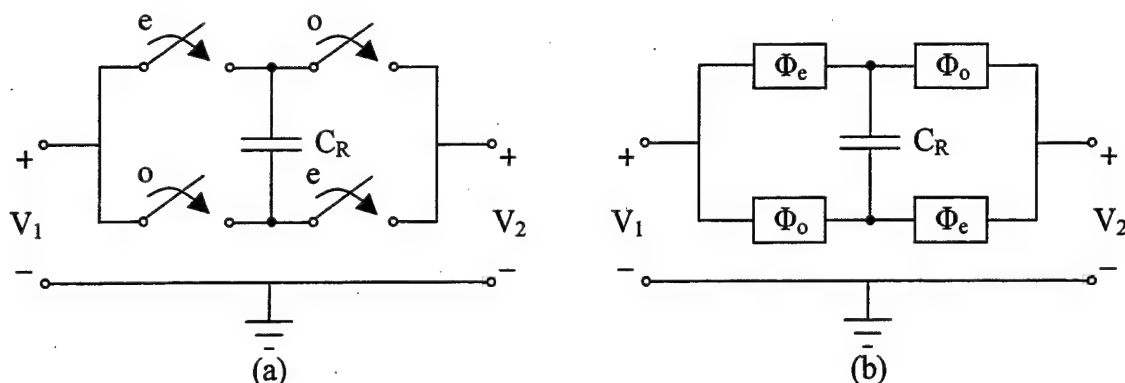
Figure 6.1: The Floating Bilinear Resistor

Ghausi and Laker [Ref. 6] have developed a novel and effective method of determining z-domain transfer functions. Their method involves substitution of z-domain equivalent circuits for the various s-domain components, then analyzing the resulting overall equivalent circuit. In developing the z-domain transfer function of the GIC filter I will use a combination of the Ghausi / Laker substitution method, along with the use of the generic admittance s-domain transfer functions developed in Chapter V.

The first step in the development is to perform the Ghausi / Laker substitution. With the use of switched-capacitor resistances all the GIC filter admittances are now either floating capacitors or FBRs. Figure 6.2 diagrams a floating capacitor, and its Ghausi / Laker z-domain equivalent.
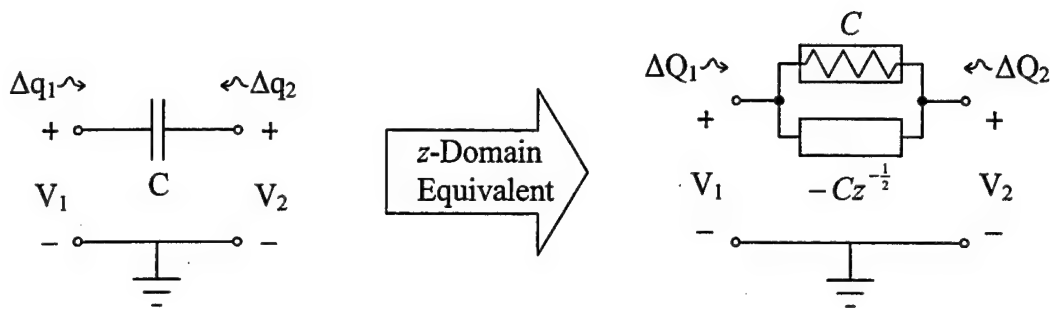
Figure 6.2: *Z*-Domain Equivalent of Floating Capacitor

Figure 6.3 shows the Ghausi / Laker z-domain equivalent of the Floating Bilinear Resistor.
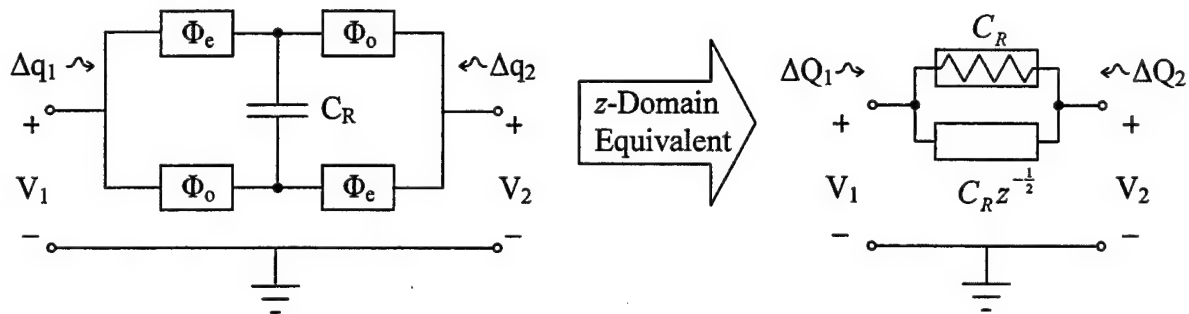
Figure 6.3: *Z*-Domain Equivalent of Floating Bilinear Resistor

It should be noted that the floating capacitor and the FBR are special cases of the Ghausi / Laker z-domain equivalent components. These two components have z-domain equivalents that are far simpler than those of other components due to symmetry of the circuits and switching.

In the z-domain equivalent circuits the block components are z-domain admittances. These admittances have magnitudes as shown, and, more importantly, are subject to the same rules as standard admittances. Specifically, admittance values in

parallel can be added to form an equivalent admittance. I will use this property to further simplify the z-domain equivalent circuits. The result is a lumped z-domain admittance for each type of component in the switched-capacitor GIC filter. These lumped z-domain admittance values can then be entered into the generic admittance transfer functions developed in Chapter V to find the full z-domain transfer function of the switched-capacitor GIC filter.

Table 6.1 shows the simplified (lumped) z-domain equivalent for each of the components of the switched-capacitor GIC filter.

S-Domain Circuit Component	**Lumped Z-Domain Equivalent Admittance**
Floating Capacitor	

Table 6.1: Lumped Z-Domain Equivalent Admittances

The GIC filter with generic admittances shown in Figure 5.2 remains the same regardless of what domain of operation is used. If continuous time analog components are used then the appropriate s-domain admittances should be entered for values Y_1 to Y_8. Equations 5.21 and 5.22 then yield the s-domain ideal transfer functions, while Equations 5.42 and 5.43 yield the s-domain non-ideal transfer functions. However, if a switched-capacitor implementation is planned, then the lumped z-domain equivalent admittances shown in Table 6.1 are entered for Y_1 to Y_8. Equations 5.21 and 5.22 then yield the z-domain ideal transfer functions, while Equations 5.42 and 5.43 yield the z-domain non-ideal transfer functions. Thus, we have developed a straightforward method for determining both the s and z domain ideal and non-ideal transfer functions of the GIC filter.

At this point examination of an example would be useful. Let the goal be to develop the information necessary to implement a switched-capacitor GIC filter. Let the filter parameters be:

High-Pass Filter
$\omega_p = 5000$ rad/s
Clocking Frequency $f_s = 1$ MHz
Quality Factor = 4
Assume Ideal Op Amps
Assume Resistive Impedance Magnitude = 1 kΩ

Then, we can use Equation 4.35 to find the magnitude of the capacitor used in the FBR to be

$$C_R = \frac{G\tau}{4} = 0.25\,nF \qquad \text{where } \tau = \frac{1}{f_s} \qquad \text{(Eq. 6.1)}$$

We can also find the magnitude of the floating capacitor to be

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$$C = \frac{1}{\omega_p R} = 0.2 \ \mu F \qquad\qquad \text{(Eq. 6.2)}$$

Then, if we refer to Table 5.1 to determine which type components are used for each admittance, but we use the z-domain equivalent admittances developed above, we find the circuit elements to be

$$Y_1 \Rightarrow \text{FBR with } C_R = 0.25 \ nF \qquad\qquad \therefore Y_1 = C_R\left(1 + z^{-\frac{1}{2}}\right)$$

$$Y_2 \Rightarrow \text{FBR with } C_R = 0.25 \ nF \qquad\qquad \therefore Y_2 = C_R\left(1 + z^{-\frac{1}{2}}\right)$$

$$Y_3 \Rightarrow \text{Floating Capacitor with } C = 0.2 \ \mu F \quad \therefore Y_3 = C\left(1 - z^{-\frac{1}{2}}\right)$$

$$Y_4 \Rightarrow \text{FBR with } C_R = 0.25 \ nF \qquad\qquad \therefore Y_4 = C_R\left(1 + z^{-\frac{1}{2}}\right)$$

$$Y_5 \Rightarrow \text{Open} \qquad\qquad\qquad\qquad\qquad \therefore Y_5 = 0$$

$$Y_6 \Rightarrow \text{FBR with } C_R = 0.25 \ nF \qquad\qquad \therefore Y_6 = C_R\left(1 + z^{-\frac{1}{2}}\right)$$

$$Y_7 \Rightarrow \text{Floating Capacitor with } C = 0.2 \ \mu F \quad \therefore Y_7 = C\left(1 - z^{-\frac{1}{2}}\right)$$

$$Y_8 \Rightarrow \text{FBR with } C_{RQ} = \frac{C_R}{Q_p} = 62.5 \ pF \quad \therefore Y_8 = \frac{C_R}{Q_p}\left(1 + z^{-\frac{1}{2}}\right)$$

Then, Equation 5.21, and the z-domain admittances, can be used to determine the z-domain transfer function of the filter.

$$T_1 = \frac{V_1}{V_i} = \frac{Y_1 Y_4 Y_5 + Y_2 Y_3 Y_7 + Y_3 Y_6 Y_7 - Y_3 Y_5 Y_8}{Y_1 Y_4 Y_5 + Y_1 Y_4 Y_6 + Y_2 Y_3 Y_7 + Y_2 Y_3 Y_8}$$

$$T_1 = \frac{0 + \left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right] + \left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right] - 0}{0 + \left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right]\left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right]\left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right] + \left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right] + \left[C_R\left(1 + z^{-\frac{1}{2}}\right)\right]\left[C\left(1 - z^{-\frac{1}{2}}\right)\right]\left[\frac{C_R}{Q_p}\left(1 + z^{-\frac{1}{2}}\right)\right]}$$

$$T_1 = \frac{C_R C^2\left(1 - z^{-\frac{1}{2}} - z^{-1} + z^{-\frac{3}{2}}\right) + C_R C^2\left(1 - z^{-\frac{1}{2}} - z^{-1} + z^{-\frac{3}{2}}\right)}{C_R^3\left(1 + 3z^{-\frac{1}{2}} + 3z^{-1} + z^{-\frac{3}{2}}\right) + C_R C^2\left(1 - z^{-\frac{1}{2}} - z^{-1} + z^{-\frac{3}{2}}\right) + \frac{C_R^2 C}{Q_p}\left(1 + z^{-\frac{1}{2}} - z^{-1} - z^{-\frac{3}{2}}\right)} \qquad \text{(Eq. 6.3)}$$

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$$T_1 = \frac{2C_R C^2 \left(1 - z^{-\frac{1}{2}} - z^{-1} + z^{-\frac{3}{2}}\right)}{\left(C_R^3 + C_R C^2 + \frac{C_R^2 C}{Q_p}\right) + \left(C_R^3 - C_R C^2 + \frac{C_R^2 C}{Q_p}\right)z^{-\frac{1}{2}} + \left(C_R^3 - C_R C^2 - \frac{C_R^2 C}{Q_p}\right)z^{-1} + \left(C_R^3 + C_R C^2 - \frac{C_R^2 C}{Q_p}\right)z^{-\frac{3}{2}}}$$

Equations 6.3 and 6.4 each represent the ideal op amp z-domain transfer function of a high-pass GIC filter. Returning to our specific example, all that remains is to enter the values of C_R, C, and Q_p. In order to demonstrate the transfer function, and the filtering circuit, a MATLAB simulation of the example was performed. Figure 6.4 shows the resulting magnitude response with a log scale x-axis, and Figure 6.5 shows the magnitude response with a linear scale x-axis. These figures clearly illustrate that the z-domain transfer function is indeed a high-pass filtering function with $\omega_p = 5 \times 10^3$ rad/s Thus, the procedure and the equations are correct. The ideal and non-ideal z-domain transfer functions of each of the filter types can be found using the same technique.

We have now demonstrated how the concepts presented in the previous chapters can be used together in order to specify and implement a switched-capacitor GIC filter, and determine its z-domain transfer function. This implementation would be suitable for integrated circuit fabrication. However, a variable parameter filter would prove to be far more useful. The next section will present the development of just such a filter design.
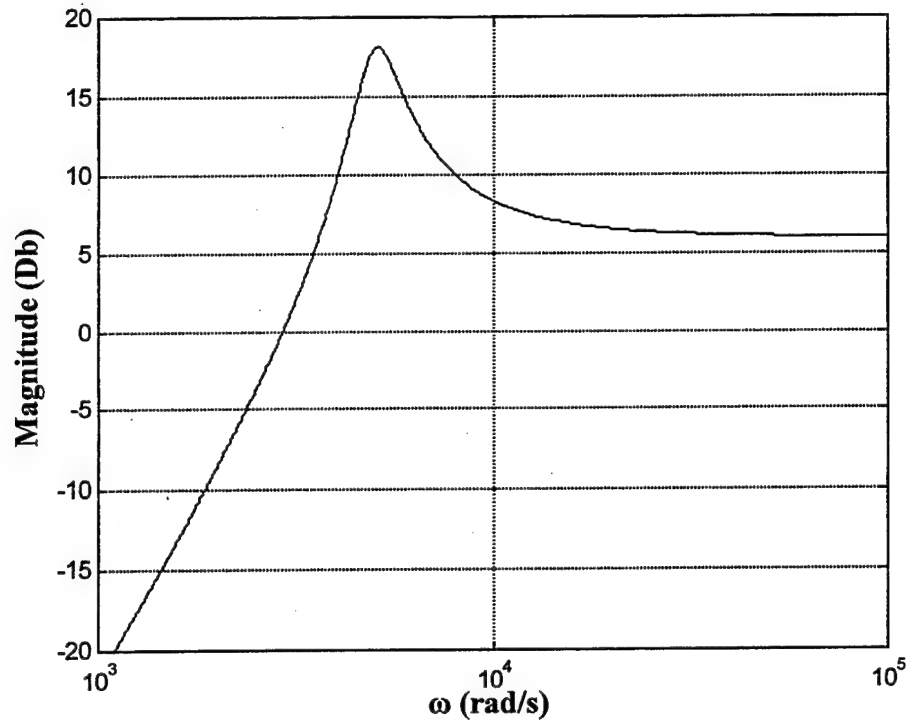
Figure 6.4: Magnitude Response of *Z*-Domain Transfer Function (x axis log scale)
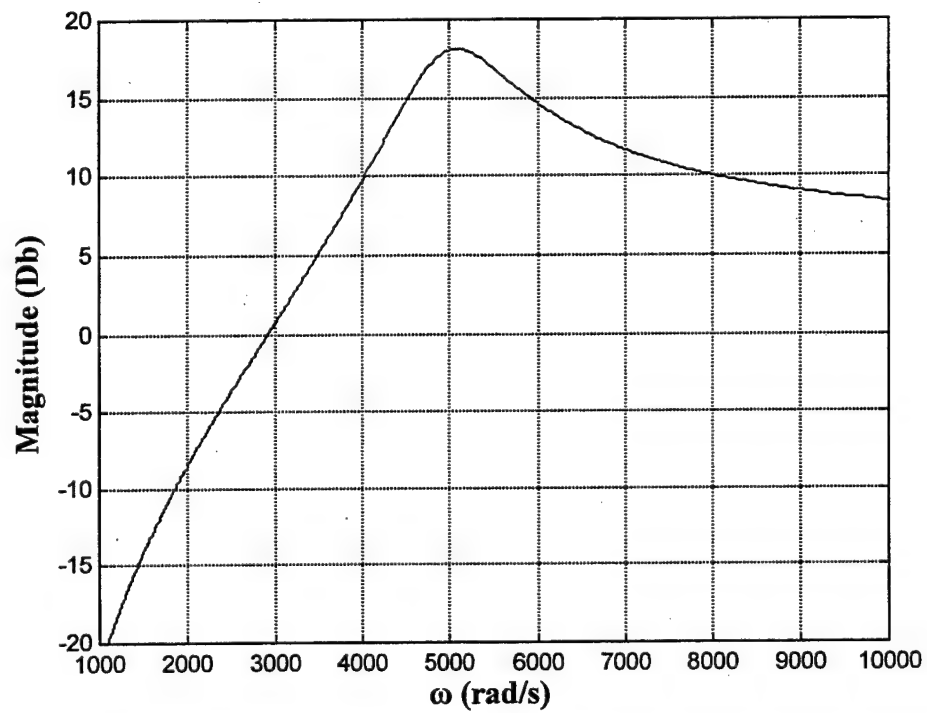
Figure 6.5: Magnitude Response of *Z*-Domain Transfer Function (x axis linear scale)

B. DIGITALLY PROGRAMMABLE GIC FILTER

In order for a filter to have maximum utility its parameters must be variable. In this project we will seek to develop a filter which is programmable (variable) in filter type (topology), center or cutoff frequency, and quality factor. Such a filter would be useful in a wide variety of roles.

The first step will be to decide how, and to what extent, the parameters of the switched-capacitor GIC filter will be varied. This filter should be able to interface with, or be controlled by, digital computer systems. Thus, digital control inputs are appropriate. Here we must again take manufacturing constraints into consideration. Often, one of the limiting factors in IC design, fabrication, and cost is the total number of input / output pins. A minimum number of pins should be used in order to keep circuit complexity and cost down. As a design choice this circuit will use an 8 bit (1 byte) control input. This will allow for several selections of each parameter, but still keep the circuit simple. Future designs could add more control bits in order to provide greater variability. The 8 bits will be divided into groups to set each of the variable parameters. Figure 6.6 shows the control byte and how it is divided to allow for selection of the parameters.
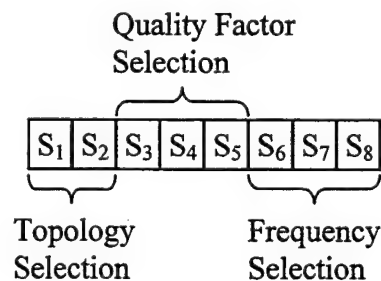
Figure 6.6: Programmable GIC Control Byte

1. Programmable Topology

It has been previously mentioned that the GIC filter can realize each of the four basic filtering types with only a small number of changes of components. To make the filter programmable we must provide all the necessary components, and a method to switch them as necessary for the desired topology. The two bits of the control word dedicated to topology selection (S_1 and S_2) allow four discrete values – one for each of the filter types. These control inputs will be used to drive a combinational logic section that controls a network of passgates. The passgates will effectively switch in and out circuit components as necessary in order to realize the four filter types. The passgates will also select the correct output node for the filter topology so that only one dedicated filter output is required. Table 6.2 shows the topology selection inputs and the corresponding filter type that is realized.

Inputs		Topology
S_1	S_2	
0	0	Notch
0	1	High Pass
1	0	Band Pass
1	1	Low Pass

Table 6.2: Filter Topology Selection

The truth table of the required topology selection logic is shown in Table 6.3

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Inputs		Topology Control Outputs																	
S_1	S_2	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18
0	0	0	1	1	0	0	1	0	0	0	1	0	1	0	1	1	0	0	1
0	1	1	0	1	0	0	1	0	0	0	1	0	1	0	1	0	1	1	0
1	0	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	1	0
1	1	0	1	0	1	1	0	0	1	0	0	1	0	1	0	0	1	0	1

Table 6.3: Topology Selection Logic Truth Table

The combinational circuitry to implement the truth table is shown in Figure 6.7.
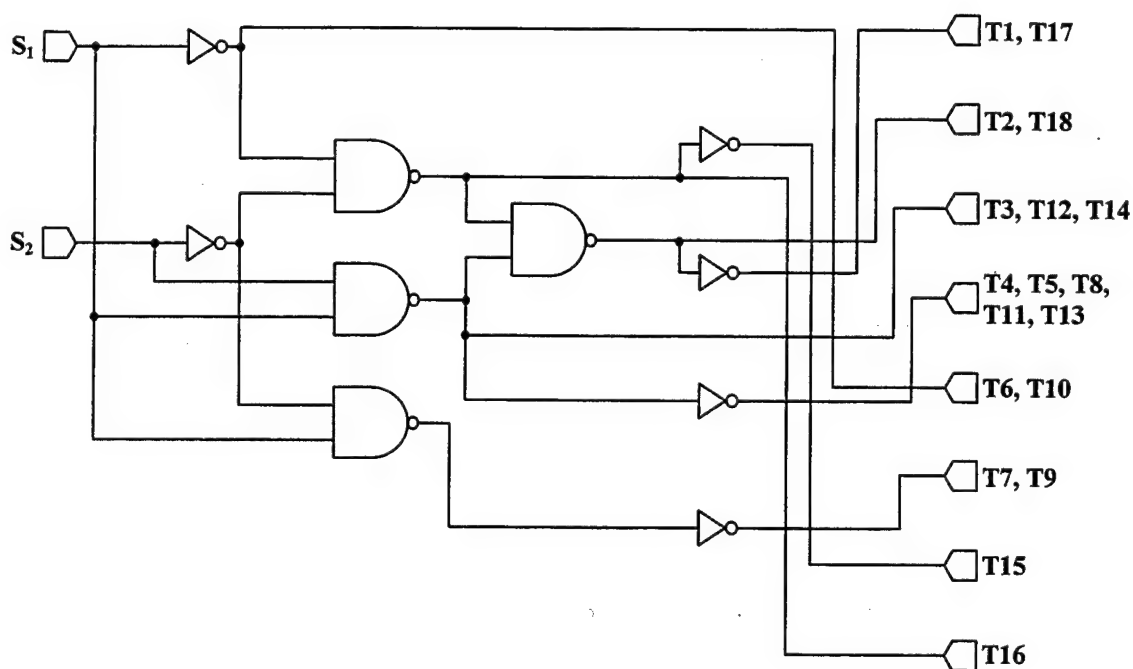
Figure 6.7: Topology Selection Logic Circuit

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Figure 6.8 shows the circuit network of the GIC filter with programmable topology. In places where a resistive admittance is needed a switched-capacitor Floating Bilinear Resistor is used. Careful examination of Figure 6.8 will show that when the circuit is controlled as indicated in Table 6.3 the correct components are realized for the various filter types. Thus we have achieved the programmability of one of the filter parameters.
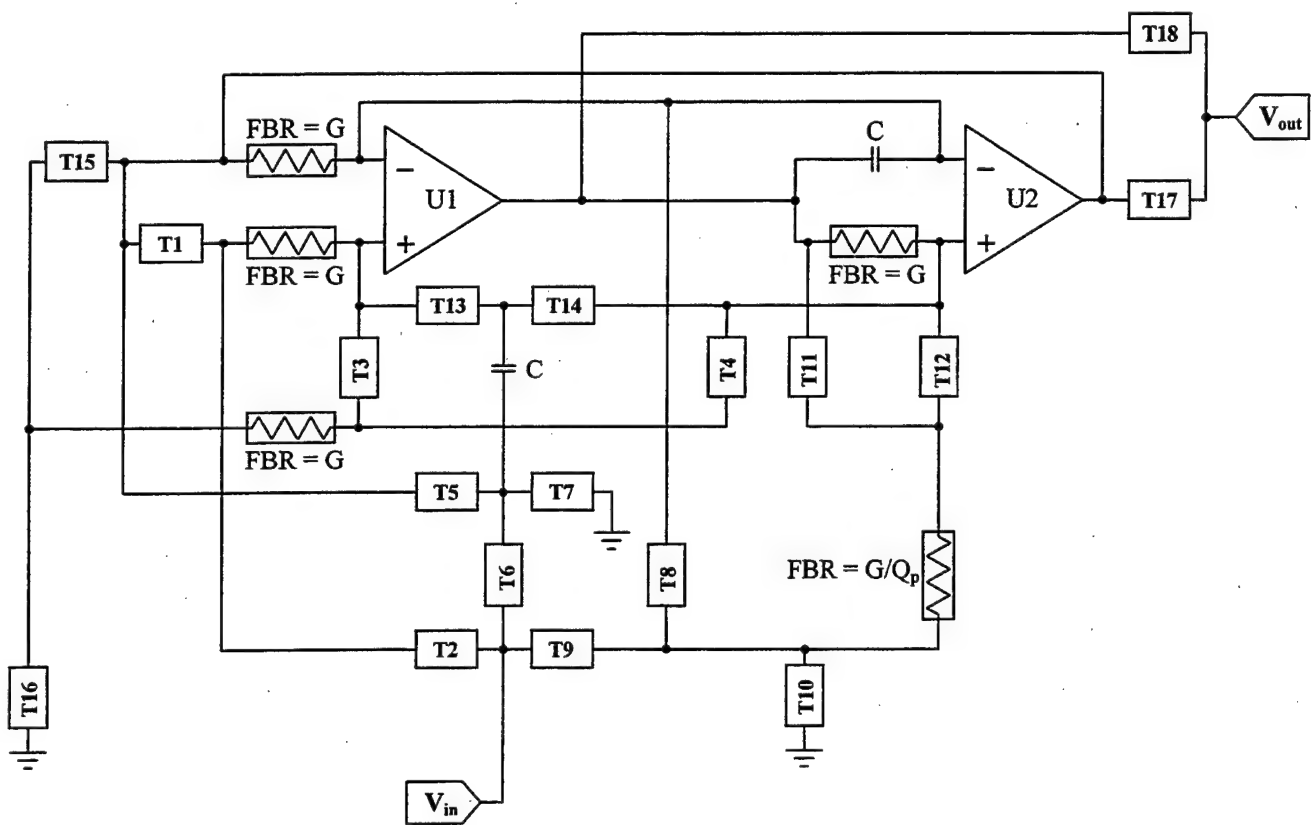
Figure 6.8: GIC Filter With Programmable Topology

2.   Programmable Frequency

The next parameter that we wish to make programmable is the filter cutoff (or center) frequency. In the GIC filter this frequency is determined by the values of the two floating capacitors. To make the filter programmable in frequency we have only to replace these capacitors with programmable capacitors. Here we will utilize the fact that capacitors in parallel can be added together to form an equivalent capacitance. By networking four capacitors in parallel, with passgate switches to control the connections, we can realize a programmable capacitance. Figure 6.9 illustrates the simple network required to implement a variable capacitor.
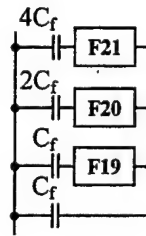
Figure 6.9: Variable Capacitor Network

In this figure the value C_f represents a unit capacitance. The passgates are now labeled F##, to indicate that they control frequency in the filter. The logic network needed to control the two variable capacitors in the filter is extremely simple. The bits of the control word which are dedicated to frequency selection (S_6, S_7, S_8) are simply buffered and sent to passgates in the two variable capacitors. Figure 6.10 illustrates this control logic.
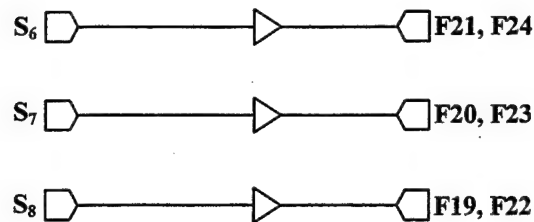
Figure 6.10: Frequency Selection Logic Circuit

The truth table of the frequency selection logic is straightforward, and is shown in Table 6.4.

Freq Selection Inputs			Frequency Control Outputs					
S_6	S_7	S_8	F19	F20	F21	F22	F23	F24
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	0	0
0	1	0	0	1	0	0	1	0
0	1	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0	1
1	0	1	1	0	1	1	0	1
1	1	0	0	1	1	0	1	1
1	1	1	1	1	1	1	1	1

Table 6.4: Frequency Selection Logic Truth Table

The unit capacitance used in this project is $C_f = 3$ nF. Table 6.5 shows the frequency selection inputs, and the resulting capacitance and cutoff (or center) frequency set by the inputs.

Freq Selection Inputs			Capacitance	Frequency
S_6	S_7	S_8		
0	0	0	3 nF	90.00 kHz
0	0	1	6 nF	51.60 kHz
0	1	0	9 nF	35.40 kHz
0	1	1	12 nF	26.55 kHz
1	0	0	15 nF	22.80 kHz
1	0	1	18 nF	18.45 kHz
1	1	0	21 nF	15.60 kHz
1	1	1	24 nF	13.95 kHz

Table 6.5: Frequency Selection Results

Then, in order to realize a GIC filter that is programmable in both topology and frequency we simply must insert the variable capacitors in place of the two floating capacitors. Once again it should be noted that if more bits are allocated for frequency selection then a greater range of frequencies, or smaller step size between values, can be achieved. The number of bits used, and the frequency selections available, in this project illustrate the concept while keeping the overall circuit relatively simple. Extension to a greater number of control bits and frequency choices is easily accomplished. Figure 6.11 illustrates the GIC filter with programmable topology and frequency.
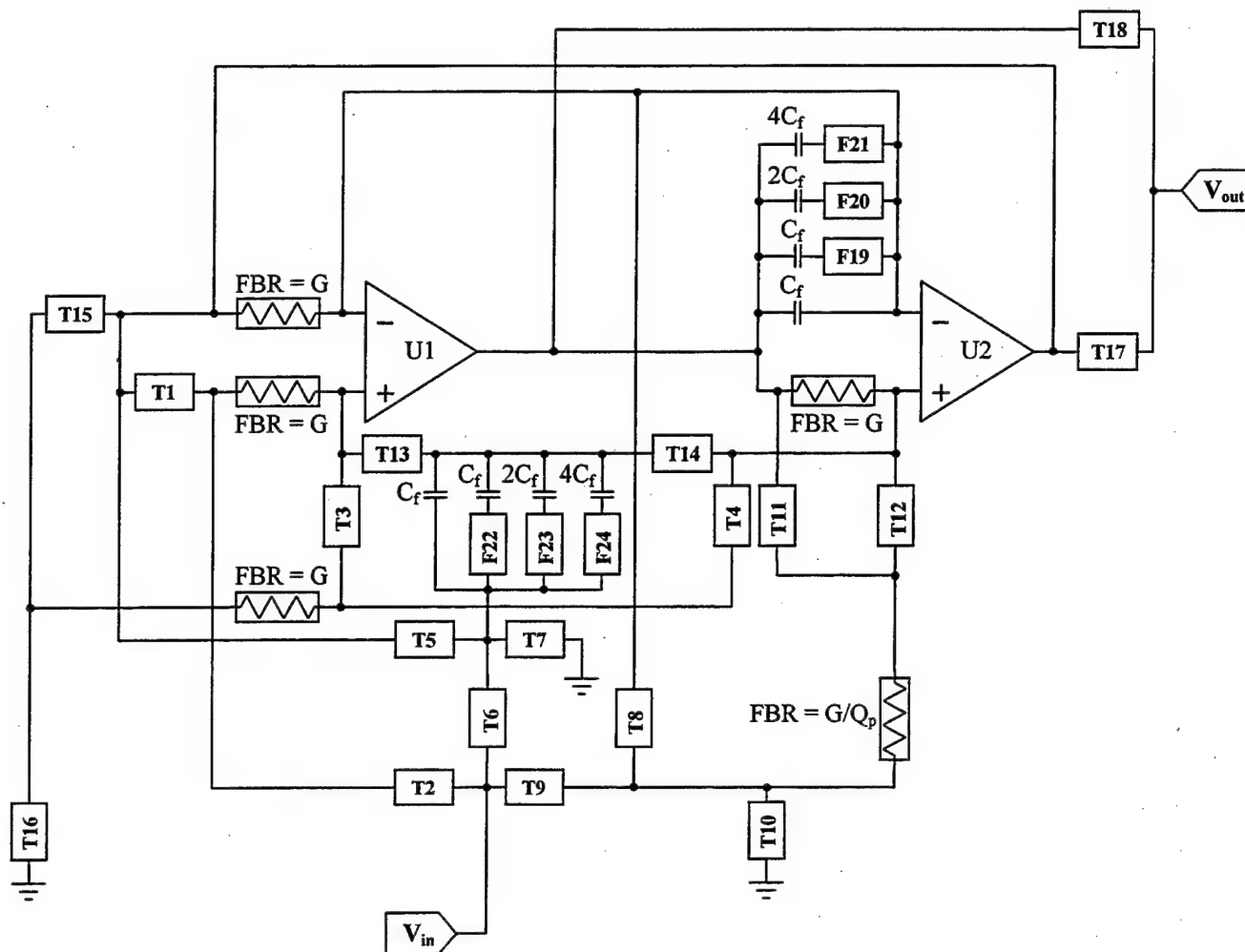
Figure 6.11: GIC Filter With Programmable Frequency and Topology

3. Programmable Quality Factor

The final parameter that we wish to make programmable in the GIC filter is

quality factor. In the GIC filter the quality factor is determined by the value of a single

resistive admittance. This allows for control of the quality factor simply by controlling

that admittance. This project utilizes switched-capacitors as resistive elements.

Therefore, a variable capacitor network, similar to that used for frequency selection, can

be used to control the quality factor as well. The simple variable capacitor network used in the frequency selection allows only integer multiples of the unit capacitance. In filtering circuits a flat magnitude response is often desired. To implement a flat magnitude response a quality factor below unity is necessary. Therefore, a slightly more complex variable capacitor system is required for quality factor programming. When this variable capacitor is combined with the passgates appropriate for a switched-capacitor admittance the result is a variable Floating Bilinear Resistor. Figure 6.12 shows the variable Floating Bilinear Resistor used for quality factor control.
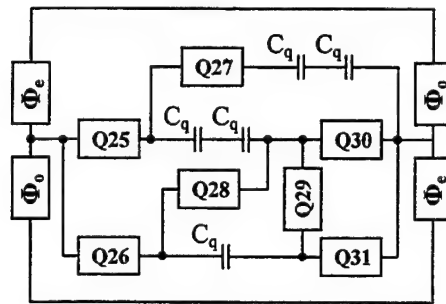
Figure 6.12: Variable FBR Network for Quality Factor Control

Table 6.6 shows the truth table of the quality factor selection logic, while Table 6.7 shows the inputs required to achieve a desired quality factor. The bit patterns associated with the various quality factors were chosen to simplify to logic necessary to control the switches. Also, with the simple variable FBR network used in this project two bit patterns of the quality factor control bits were not needed. These bit patterns are available for future use, as indicated in Table 6.7.

QF Selection Inputs			Quality Factor Control Outputs						
S$_3$	S$_4$	S$_5$	Q25	Q26	Q27	Q28	Q29	Q30	Q31
0	0	0	0	1	1	0	1	0	0
0	0	1	0	1	1	1	1	0	0
0	1	0	0	1	0	0	0	0	1
0	1	1	0	1	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0
1	0	1	1	0	0	1	1	1	0
1	1	0	1	0	0	0	0	0	1
1	1	1	1	0	0	1	0	0	1

Table 6.6: Quality Factor Logic Truth Table

QF Selection Inputs			Filter Quality Factor
S$_3$	S$_4$	S$_5$	
0	1	1	0.8
0	1	0	1
1	0	0	2
1	1	1	3
0	0	1	4
0	0	0	5
1	0	1	Future Use
1	1	0	Future Use

Table 6.7: Filter Quality Factor

The combinational logic needed to control the filter quality factor is shown in Figure 6.13.
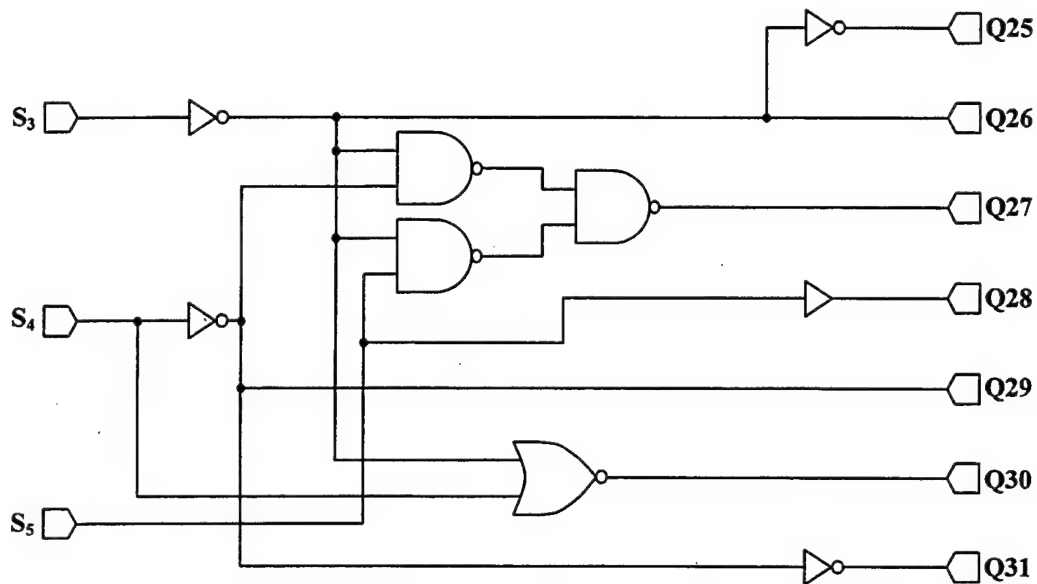
Figure 6.13: Quality Factor Selection Logic Circuit

Then, if we include the variable FBR for quality factor control in the GIC filter
we have developed previously, we have the desired GIC filter with programmable
topology, frequency, and quality factor. Figure 6.14 shows the circuit diagram for this
filter.

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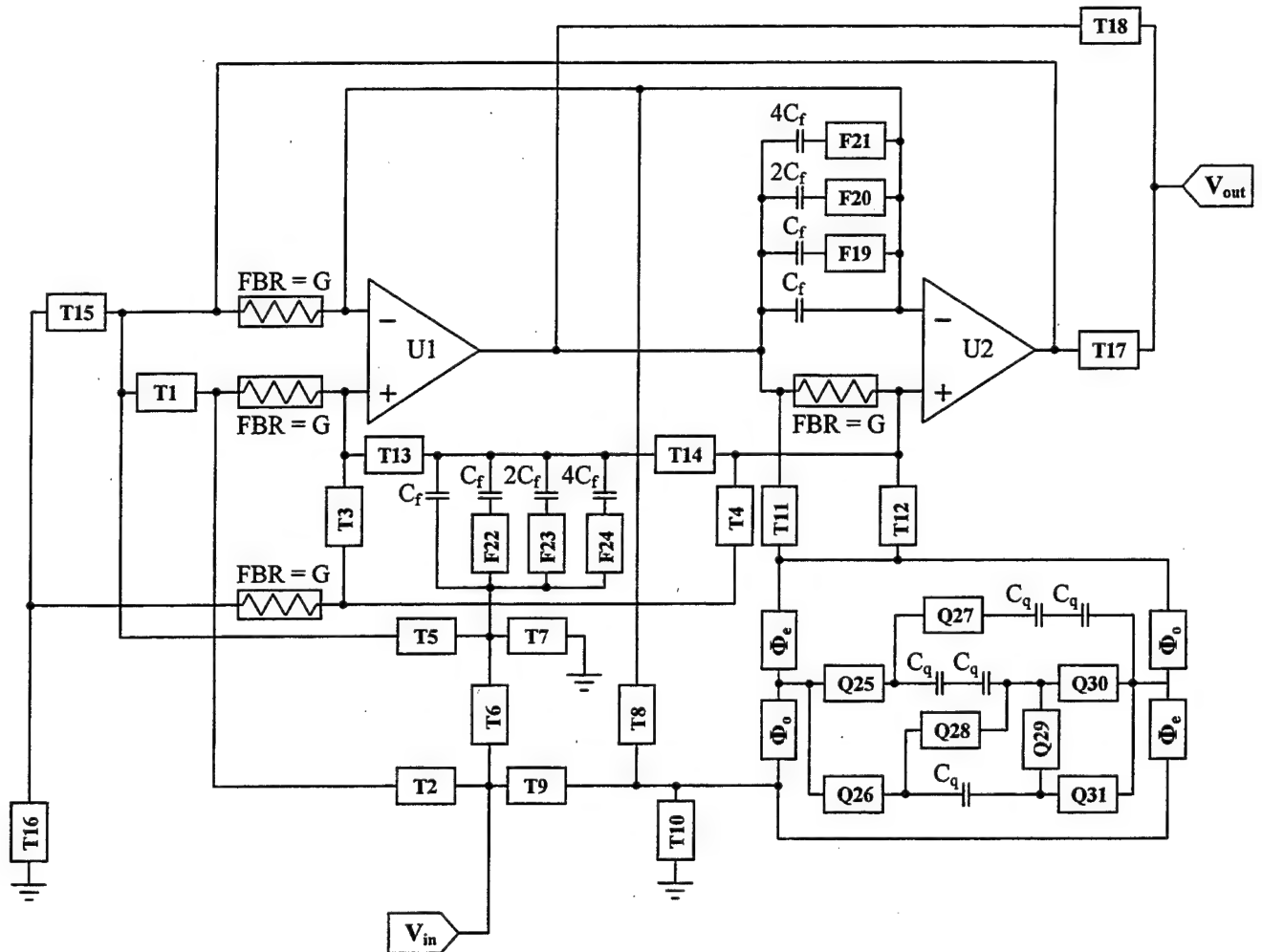
Figure 6.14: GIC Filter With Programmable Frequency, Topology, and Quality Factor

Thus, by integrating the GIC filter network, switched-capacitor resistances, digital control logic, and the strengths of modern IC fabrication, we have developed the circuit which was the goal of this project – an accurate, digitally programmable, analog-to-analog filter which is variable in topology, frequency, and quality factor. Figure 6.15

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shows the complete circuit diagram for this filter, including the switched-capacitor resistances. The next chapter will deal with the VLSI implementation of this design.

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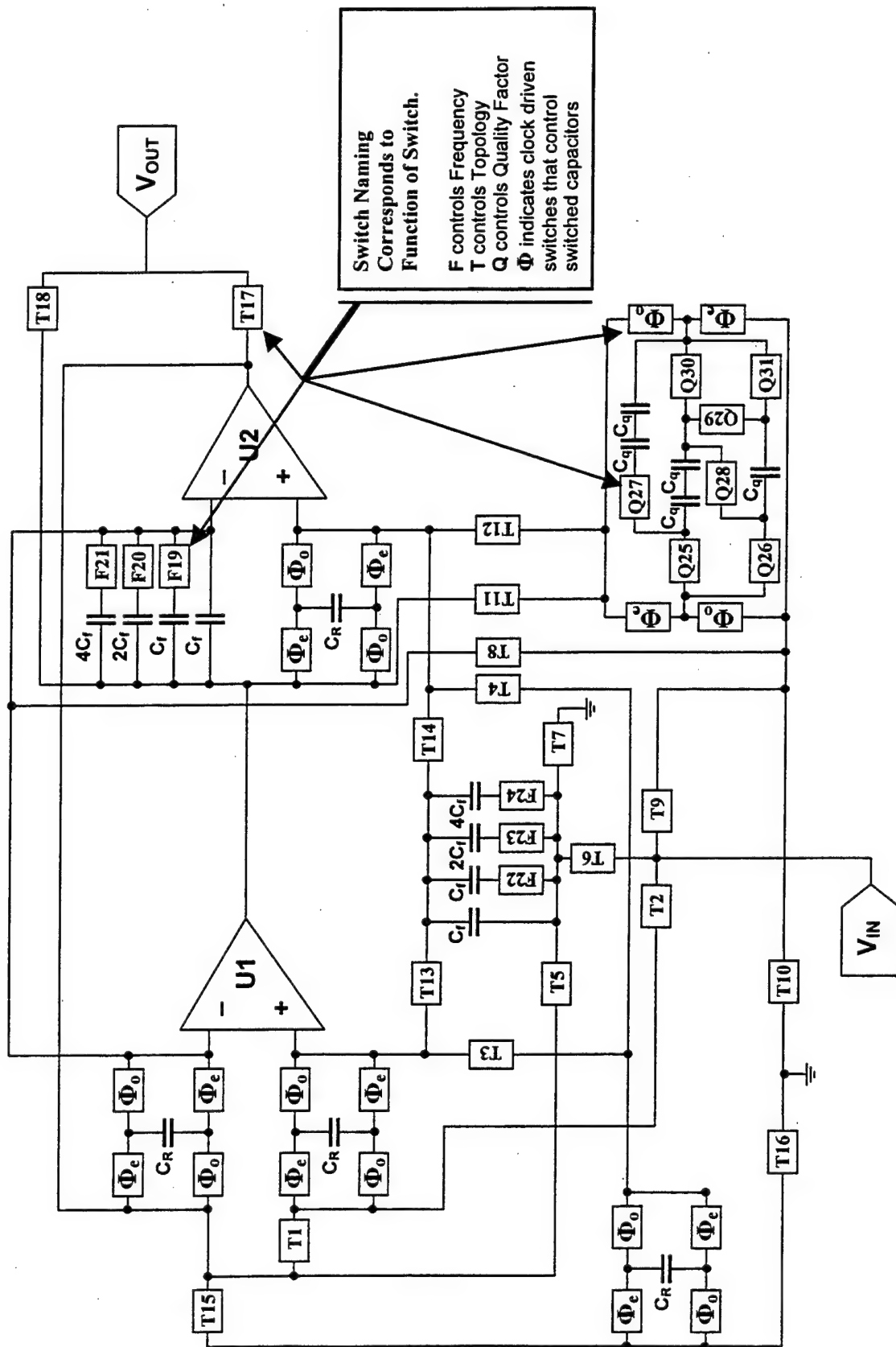
Figure 6.15: Complete GIC Filter With Programmable Frequency, Topology, and Quality Factor

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VII. VLSI IMPLEMENTATION

The final step in the design of the programmable GIC filter is to determine the Very Large Scale Integration (VLSI) implementation. The design considerations of this chapter combine all facets of the previous chapters, and add to them consideration of IC fabrication techniques and limitations imposed by the particular fabrication method available for this project.

A. DESIGN TOOLS AND FABRICATION METHOD

The design tool used in this project was the Cadence integrated circuit development software suite. The Cadence software suite is a complicated system, but represents the state of the art in integrated circuit development at the time of this project. There are several required steps in the creation of a new design or custom IC when using the Cadence software. These steps are:

- ▶ Create a library

- ▶ Create a cell category

- ▶ Create a new schematic design using the Composer tool

- ▶ Create a symbol using the Composer tool

- ▶ Simulate the schematic design using Spectre

- ▶ Create the circuit layout using Virtuoso

- ▶ Perform a design rule check

- ▶ Create an extracted version of the layout

- ▶ Cross check the layout with the schematic

- ▶ Simulate the layout using Spectre

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All of these steps were conducted for each component and functional element in the design. The final products, the circuit layouts of each component, are shown in Appendix B. The procedure used to perform each of these steps is detailed in Ref. [11]. Additional information regarding the basics of VLSI design is also contained in Ref. [3].

Integrated circuit design must also take into account the planned methods of fabrication. The circuit of this project has been designed for fabrication using the MOSIS scalable CMOS design technology. The MOSIS scalable CMOS design rules specify a twin-tub process with drawn feature sizes ranging from 2.0 μm down to 0.6 μm. Other features of the MOSIS scalable CMOS design technology include three layers of metal, and two layers of poly-silicon. The dual layers of poly-silicon are very useful in the production of IC capacitors. Reference [12] contains the complete specification of the MOSIS scalable CMOS design rules.

B.   VLSI LAYOUT

1.   Low Level Cells
The first step in the VLSI implementation of the design was the construction of several low level cells. These low level cells could then be used throughout the design. Table 7.1 lists the low level cells which were developed, and their functions. Brief descriptions of the nine cells are included below.

▶ **inv_log:** This is the standard logic inverter in this design. This inverter is used throughout the logic sections, and anywhere a general purpose inverter is required.

▶ **inv_c1:** This inverter is used at the input of the two phase clock circuit. It is similar in design to inv_log.

▶ **inv_c2:** This inverter is used within the two phase clock circuit. It features wider gates than inv_c1.

► **inv_c3:** This inverter is used at the output of the two phase clock circuit. It achieves larger effective gate widths through a multi-finger design in order to provide increased drive capability.

► **passgate:** This is a standard passgate. It consists of minimum size n and p FETs, and is used to implement the switching in the switched capacitors.

► **passgate_si:** This is a "single input" passgate. Here "single input" means that the gate requires only the control signal, not the complement of the control signal. This gate is a combination of an inverter and a passgate.

► **buffer:** This is a standard logic buffer. It consists of two inverters connected in series. It is used in the frequency logic section, and anywhere a buffer is needed.

► **nand2:** This is a standard 2 input NAND gate. It is used throughout the logic subsections.

► **nor2:** This is a standard 2 input NOR gate. It is used within the two phase clock circuit, and throughout the logic subsections.

Cell Name	Function
inv_log	Logic Inverter
inv_c1	Inverter used in the clock circuit
inv_c2	Inverter used in the clock circuit
inv_c3	Inverter used in the clock circuit
passgate	Passgate
passgate_si	Single Input Passgate (does not require control signal complement)
buffer	Standard Buffer
nand2	Standard 2 Input NAND Gate
nor2	Standard 2 Input NOR Gate

Table 7.1: Low Level Cells Used in Design

A SPICE transient analysis of each of the low level cells was performed in order to determine their operating characteristics. The transient analysis simulated each of the cells with no load, a one inverter load, and a 100 fF load. Table 7.2 shows the results of this analysis. All of the entries given in the table are in nano-seconds.

Cell	No Load				1 Inverter Load				100fF Load			
	T_R	T_F	T_{PLH}	T_{PHL}	T_R	T_F	T_{PLH}	T_{PHL}	T_R	T_F	T_{PLH}	T_{PHL}
inv_log	0.40	0.30	0.20	0.25	0.65	0.65	0.35	0.40	1.45	1.35	0.75	0.85
inv_c1	0.20	0.15	0.10	0.15	0.45	0.40	0.25	0.30	1.05	1.15	0.60	0.80
inv_c2	0.35	0.40	0.25	0.30	0.45	0.50	0.30	0.35	0.75	0.80	0.45	0.60
inv_c3	0.45	0.30	0.15	0.15	0.50	0.35	0.25	0.20	0.60	0.55	0.40	0.40
passgate	0.90	0.45	0.10	0.15	1.40	0.95	0.30	0.30	3.50	2.20	0.90	0.90
passgate_si	0.30	0.25	0.05	0.05	1.00	0.60	0.20	0.20	2.60	1.80	0.80	0.80
buffer	0.45	0.40	0.65	0.65	0.70	0.65	0.80	0.80	1.50	1.40	1.20	1.20
nand2	0.25	0.25	0.15	0.20	0.45	0.70	0.25	0.45	1.25	2.10	0.70	1.15
nor2	0.25	0.20	0.20	0.15	0.85	0.40	0.45	0.30	2.55	1.25	1.25	0.80

Table 7.2: Low Level Cell Transient Characteristics

The layouts of each of the low level cells are shown in Appendix B. The next step in the process was the development of the functional blocks of the GIC filter.

2.   GIC Functional Blocks

Once the design of the low level cells was complete they were used to develop the functional blocks of the GIC filter. The functional blocks required to implement the GIC filter are listed below:

▶ Two Phase Clock

▶ Bilinear Switched Capacitors (Floating Bilinear Resistors)

▶ Frequency Selection Logic

▶ Quality Factor Logic

▶ Topology Selection Logic

▶ Variable Capacitor #1 & #2

▶ Op Amp #1 & #2

Figure 7.1 shows the floorplan of the GIC filter, and the required functional blocks. The layouts of each of the functional blocks are shown in Appendix B.
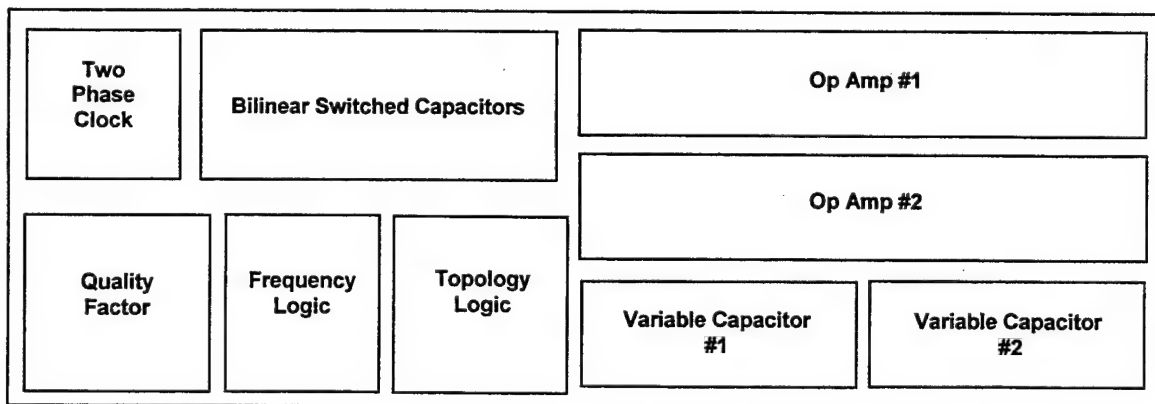
Figure 7.1: GIC Filter Block Diagram and Floorplan

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3. Chip Floorplan and Operation

The chip area available in the MOSIS process allowed for the placement of multiple GIC filters on the same chip. It was decided that two independent GIC filters would provide the greatest utility. These filters could be used individually, or cascaded to produce a higher order filtering function. With two fully programmable GIC filters on the chip there was still open area remaining; however, there were not enough pins available for another filter. The most critical elements in GIC filters are the op amps. Therefore, two additional op amps were included on the chip. These op amps have inputs and outputs which are independent of the filtering circuits. Thus, the extra op amps can be used to determine the operating characteristics, specifically the unity gain bandwidth, of the op amps internal to the filters.

The floorplan and pad assignment of the overall chip design are shown in Figure 7.2. Table 7.3 provides an explanation of the function of each of the pads used on the chip.

PAD Vdd	S3 A	CLK A	IN A	Digital Vdd A	Digital GND A	OUT A	S6 A	S7 A	S8 A	PAD Vdd
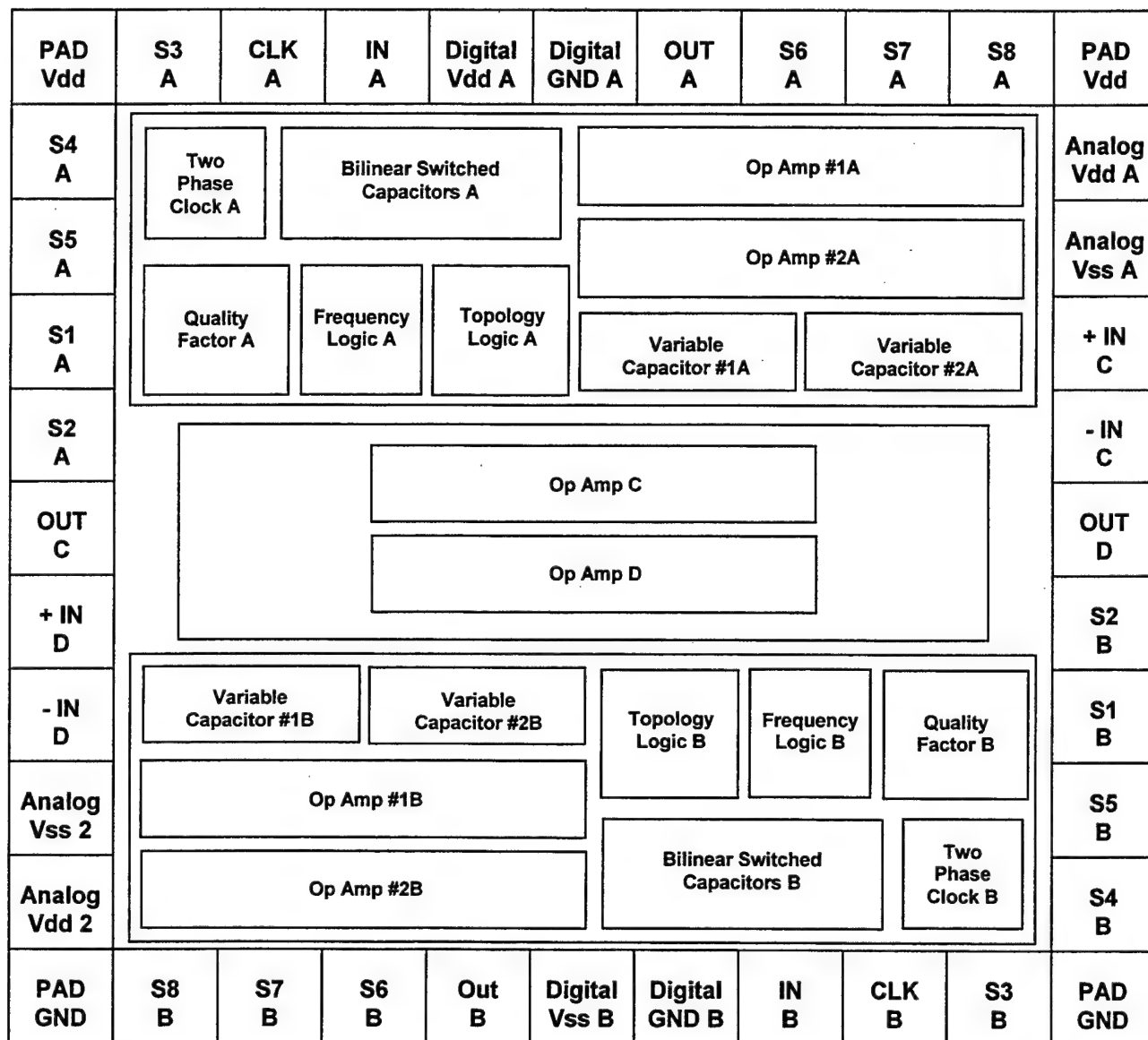
Figure 7.2: Overall Chip Floorplan and Pad Assignments

Pad Name	Function
PAD Vdd (2)	Provide power to the pad ring
PAD GND (2)	Provide ground to the pad ring
CLK A	Clock input for GIC Filter A
IN A	Input of GIC Filter A
OUT A	Output of GIC Filter A
S1 A → S8 A	Selection Inputs for GIC Filter A (Control of Filter Parameters)
Digital Vdd A	Provide power for digital portions of GIC Filter A
Digital GND A	Provide ground for digital portions of GIC Filter A
Analog Vdd A	Provide V_{dd} voltage for analog portions of GIC Filter A, and Op Amp C
Analog Vss A	Provide V_{ss} voltage for analog portions of GIC Filter A, and Op Amp C
+ IN C, - IN C	The inputs for Op Amp C
OUT C	The output of Op Amp C
+ IN D, - IN D	The inputs for Op Amp D
OUT D	The output of Op Amp D
CLK B	Clock input for GIC Filter B
IN B	Input of GIC Filter B
OUT B	Output of GIC Filter B
S1 B → S8 B	Selection Inputs for GIC Filter B (Control of Filter Parameters)
Digital Vdd B	Provide power for digital portions of GIC Filter B
Digital GND B	Provide ground for digital portions of GIC Filter B
Analog Vdd B	Provide V_{dd} voltage for analog portions of GIC Filter B, and Op Amp D
Analog Vss B	Provide V_{ss} voltage for analog portions of GIC Filter B, and Op Amp D

Table 7.3: Explanation of Pad Functions

Operation of the chip is relatively straightforward. The first step in testing or use is to provide power and ground to the appropriate pads. Both pads marked **Digital Vdd**, and both those marked **PAD Vdd**, should be connected to a +5 volt power supply. Both pads marked **Digital GND**, and both those marked **PAD GND**, should be connected to ground. The two pads marked **Analog Vdd** should be connected to +15 volt power supply, and those marked **Analog Vss** should be connected to –15 volts.

With these connections made the test op amps (C & D) can be used. The inputs and outputs of these op amps are shown in the floorplan diagram. The op amps function in the same manner as standard op amps, and can be used to determine the characteristics of the op amps within the filters.

To utilize the GIC filters a clock signal must be supplied. The GIC filters have independent clock inputs (**CLK A & CLK B**), each of which should be connected to a 1 MHz clock signal. Variation of the clock signals from the 1 MHz value will alter the effective resistances of the switched capacitors in the filter. The filter should continue to function at different clock rates; however, due to potential warping effects, the clock frequency should be kept approximately 10 times that of the filter corner frequency

Once all the power, ground, and clock inputs are supplied the GIC filters may be used. The selection inputs (**S1** → **S8**) of each of the two GIC Filters must be set to either ground or +5 volts according to the desired filter characteristics detailed in Chapter 6. At this point the filter is ready to receive input and generate output. The two GIC filters may be used independently, or may be cascaded through external connections to realize higher order filtering functions.

The magnitude responses of the programmable GIC filter are shown in Appendix A. The next chapter will deal with the conclusions and recommendations from this project.

VIII. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The overall goal of this research was to develop the design and implementation of a digitally programmable, analog-to-analog, GIC filter, which was suitable for integrated circuit fabrication. Such a filter would be useful in a wide range of applications, including communications, control systems, and signal processing. This project has been the continuation of research into the area of integrated circuit, digitally programmable filters.

The design of this project has been based on the Generalized Impedance Converter filter circuit. This circuit provided two major benefits. First, it was capable of simulating inductive impedances. Thus, by using the GIC filter, one of the components which is troublesome to manufacture in integrated circuit form was eliminated. This was a major step towards the development of an overall design suitable for IC fabrication. The second benefit of the GIC filter is its ability to realize any of the four basic filter types with only a small number of component changes. This characteristic allowed for the development of a programmable design through the use of passgates controlling the various components of the filter.

Switched capacitors provided the next step toward the IC design. Fabrication of accurate integrated circuit resistors is difficult and costly. By using switched capacitors to realize resistive impedances the problematic IC resistors were eliminated.

Once the overall circuit design had been completed there was a need to develop a method for determining the filter transfer function. This research presented a simple and effective way to do this by combining the concept of z-domain equivalent circuits, and s-

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domain generic admittance transfer functions. This method will provide future designers with the ability to rapidly determine GIC filter transfer functions, and the component values necessary to implement the transfer functions.

The overall circuit of this project was successfully designed and simulated. Appendix A contains the magnitude responses of the filter for its various programming settings. As shown in this appendix, the filter is indeed variable in topology, quality factor, and frequency. The range of available quality factors, and the range and spacing of frequency selections, are a direct result of the number of control bits allocated to programmability. The eight bits used for programmability in this project allow a demonstration of the filter capabilities, while keeping the overall circuit relatively simple. An increase in the number of control bits would allow a greater number of quality factors, and a greater range and finer spacing of frequency selections. Appendix B shows the VLSI layouts of the components necessary to implement the design as outlined and floorplanned in Chapter VII.

B.   RECOMMENDATIONS

This research has furthered the programmable GIC filter design. Errors in previous designs have been corrected, and a new method for determining the transfer function has been developed. The next logically step is the actual IC fabrication and testing of the design. This could be the starting point for future work.

Investigation of the GIC filter circuit sensitivity to stray capacitance is also warranted. The unique GIC design provides a very low sensitivity to most component variations. Research into the effects of stray capacitance could verify that the design is stray insensitive, thus further proving the utility of the design.

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Future design efforts could also include the use of composite operational amplifiers in the circuit to increase performance. Composite op amps provided increased gain-bandwidth product, and are realized simply by substituting for standard op amps in the circuit design.

There are numerous aspects of the programmable GIC filter design which warrant additional research. This area should continue to be studied, and this design further refined, for both research value and practical application.

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APPENDIX A. GIC FILTER MAGNITUDE RESPSONSE

A.   LOW-PASS FILTERING

1.   Low-Pass Filter, Quality Factor = 0.8, All Frequencies
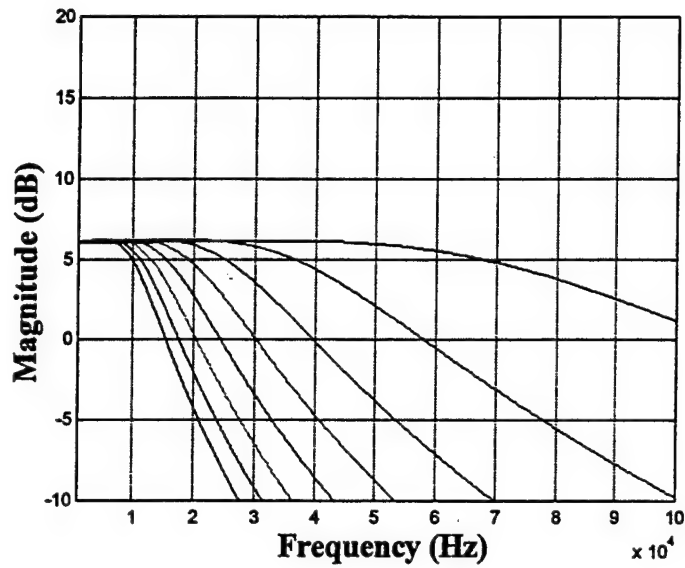
2.   Low-Pass Filter, Quality Factor = 1, All Frequencies
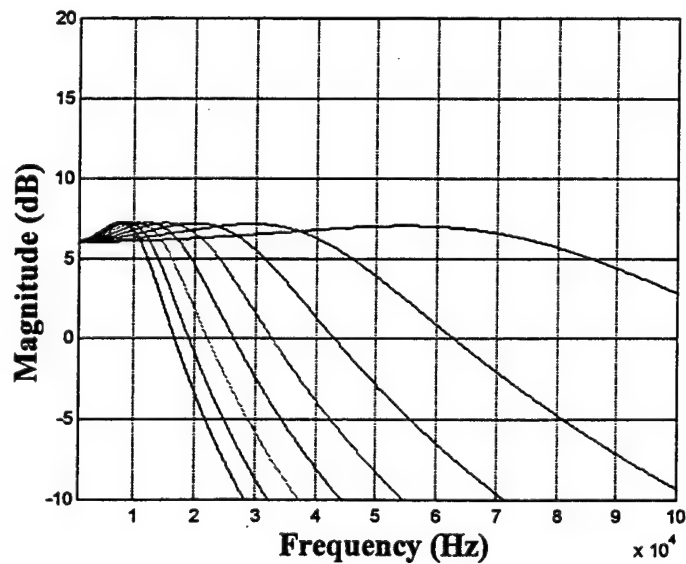
3. **Low-Pass Filter, Quality Factor = 2, All Frequencies**
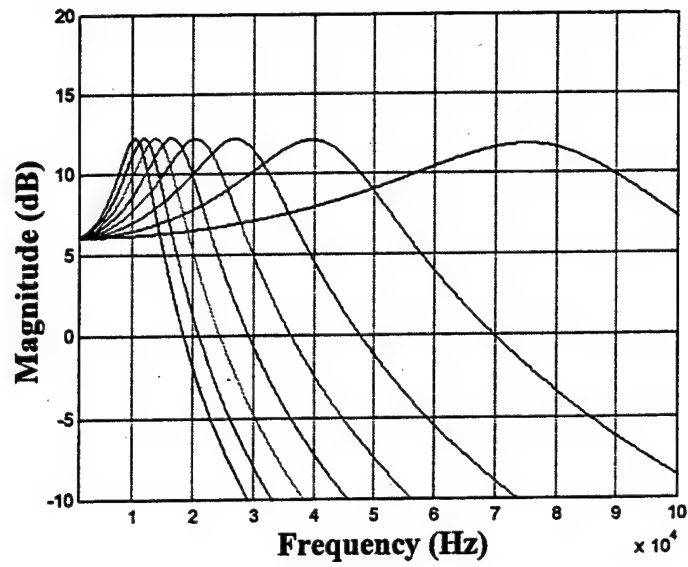
4. **Low-Pass Filter, Quality Factor = 3, All Frequencies**
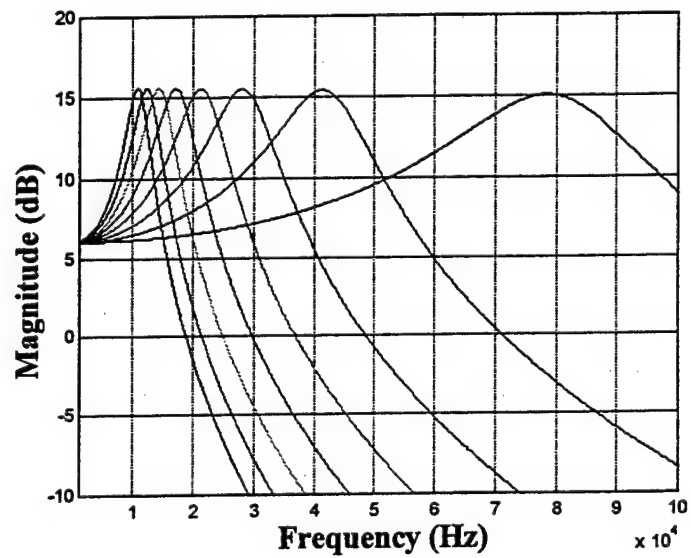
5.   Low-Pass Filter, Quality Factor = 4, All Frequencies
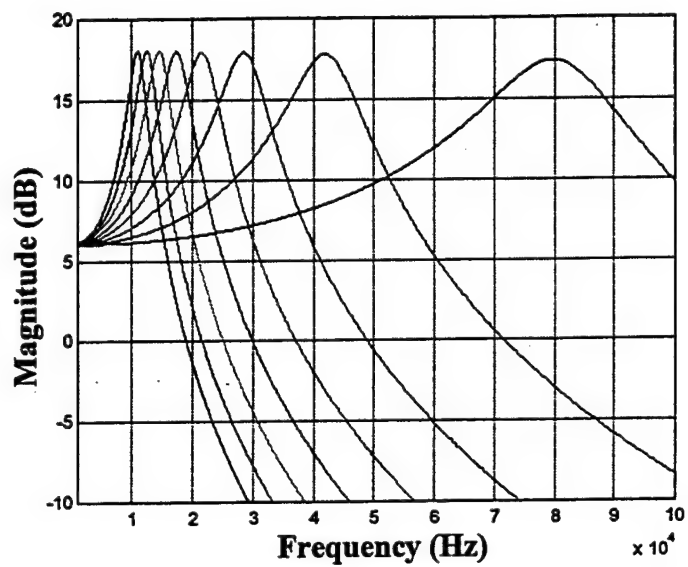
6.   Low-Pass Filter, Quality Factor = 5, All Frequencies
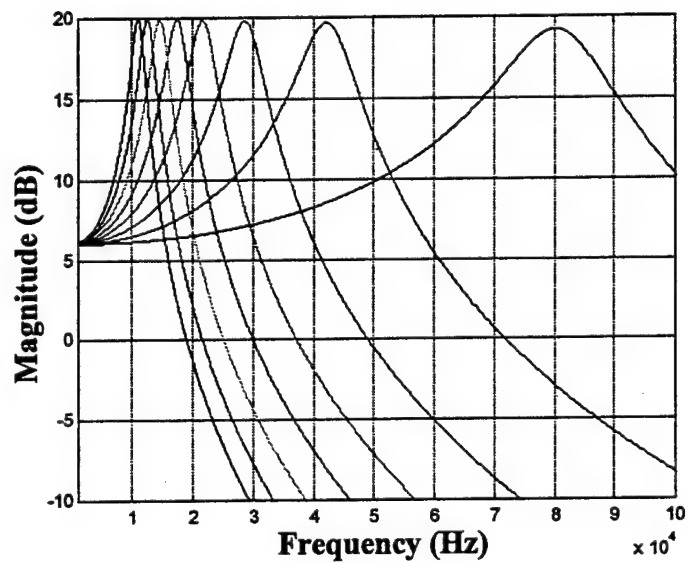
7. **Low-Pass Filter, Frequency = 90.00 kHz, All Quality Factors**
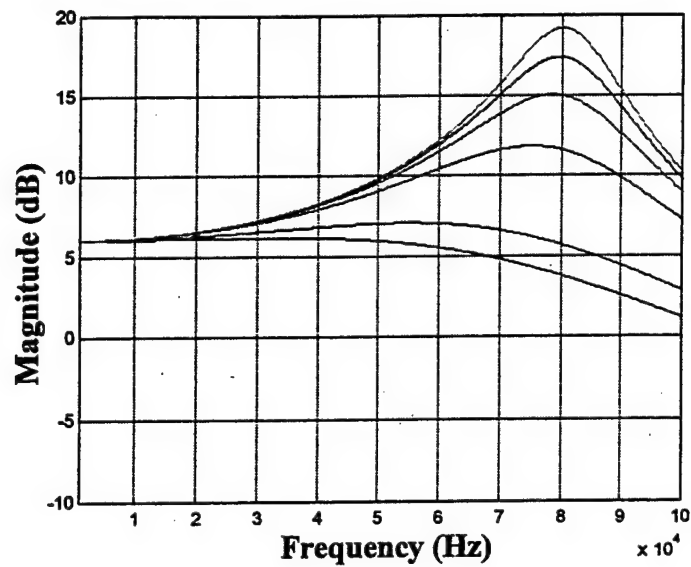
8. **Low-Pass Filter, Frequency = 51.60 kHz, All Quality Factors**

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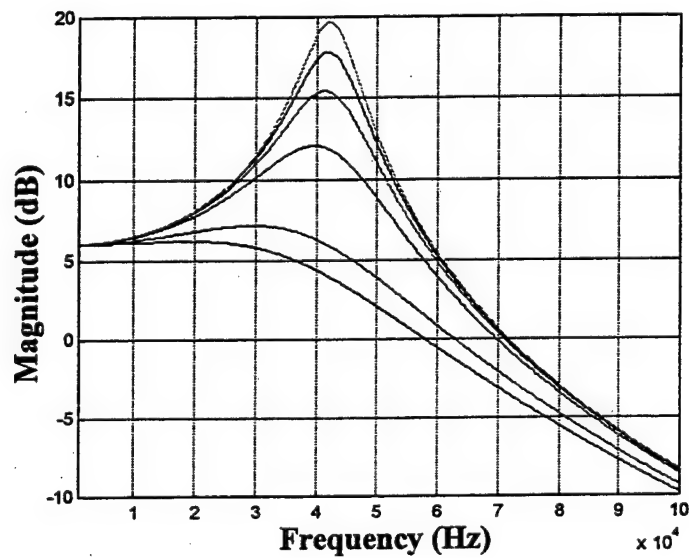
9. **Low-Pass Filter, Frequency = 35.40 kHz, All Quality Factors**
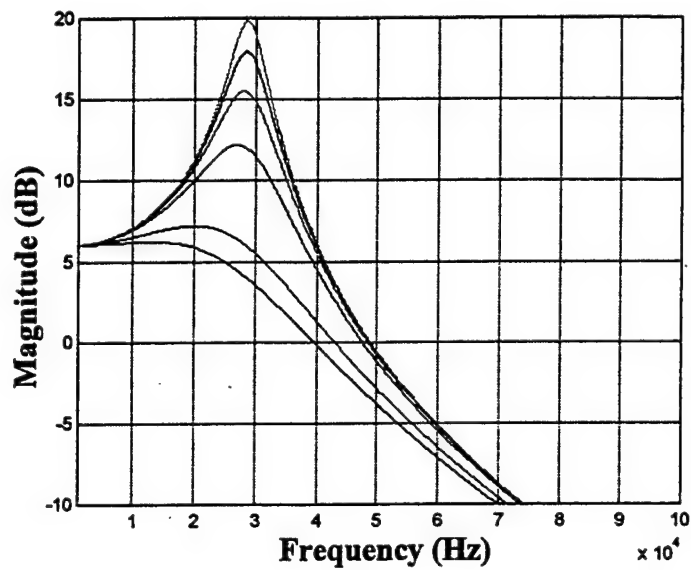
10. **Low-Pass Filter, Frequency = 26.55 kHz, All Quality Factors**

95
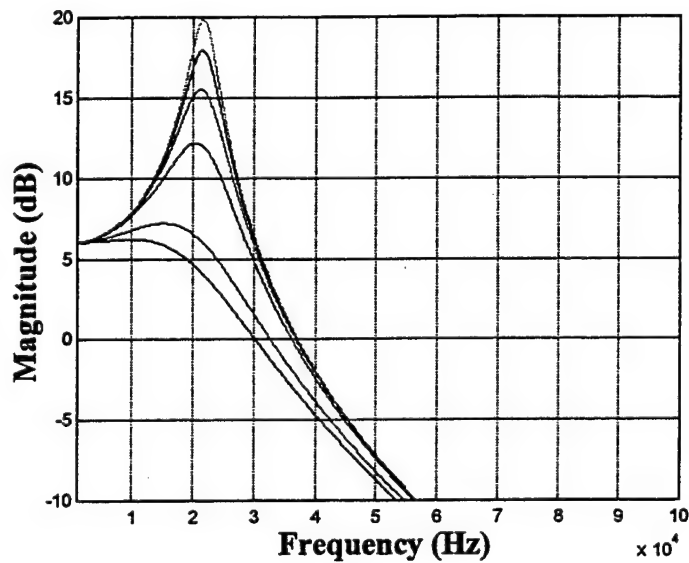
11.   Low-Pass Filter, Frequency = 22.80 kHz, All Quality Factors
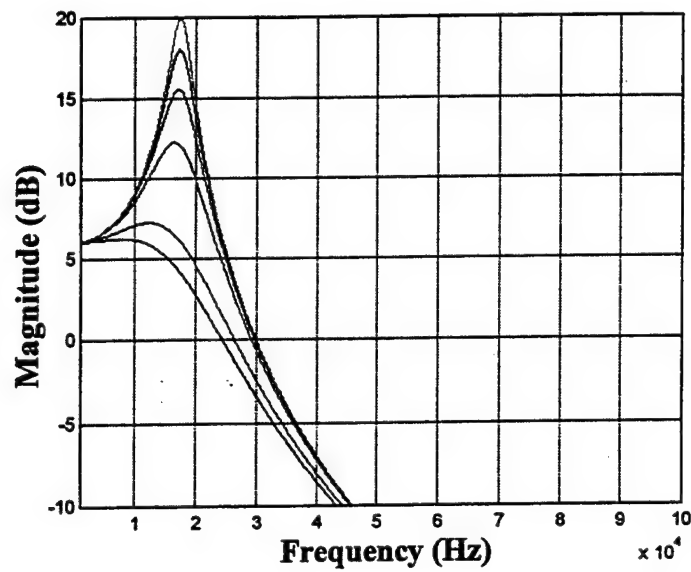
12.   Low-Pass Filter, Frequency = 18.45 kHz, All Quality Factors
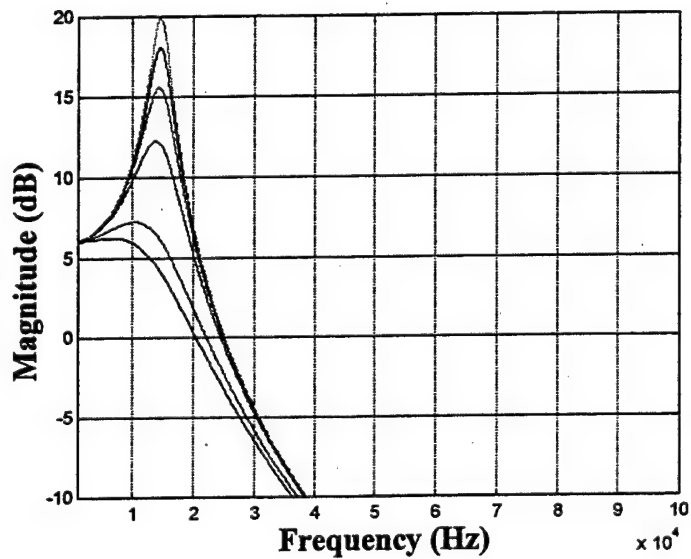
13.   Low-Pass Filter, Frequency = 15.60 kHz, All Quality Factors
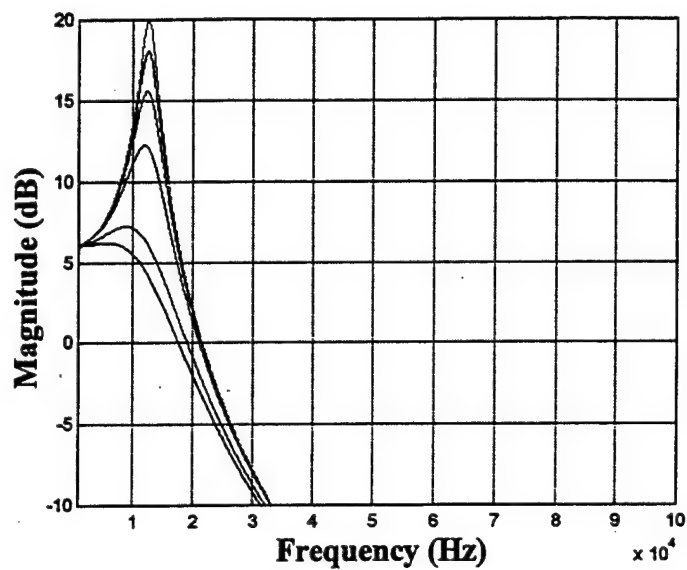
14.   Low-Pass Filter, Frequency = 13.95 kHz, All Quality Factors
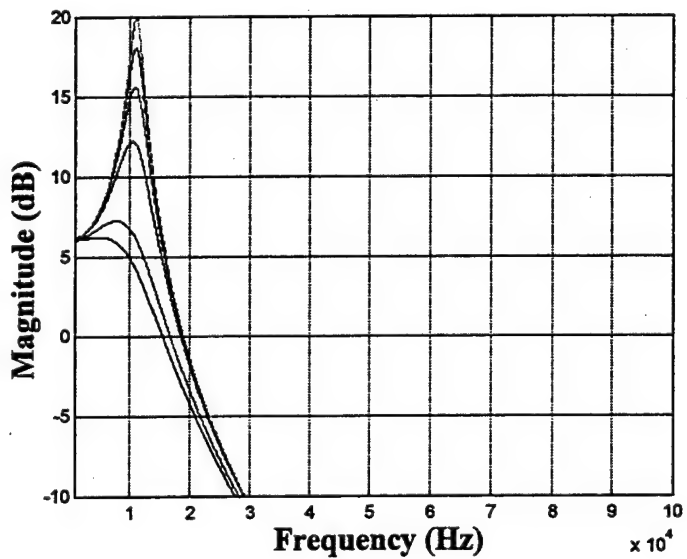
B.   HIGH-PASS FILTERING

1.   High-Pass Filter, Quality Factor = 0.8, All Frequencies
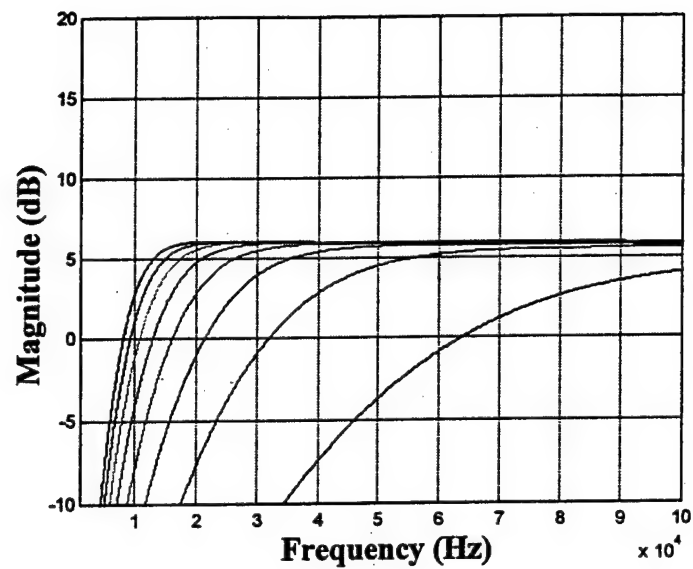
2.   High-Pass Filter, Quality Factor = 1, All Frequencies
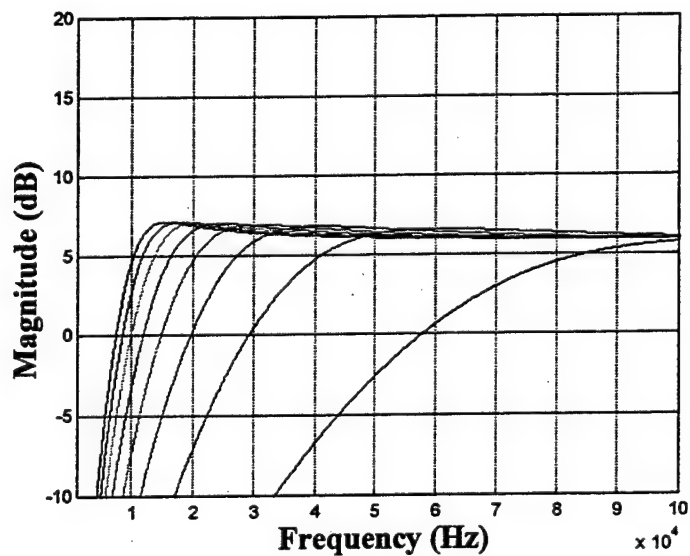
3. **High-Pass Filter, Quality Factor = 2, All Frequencies**
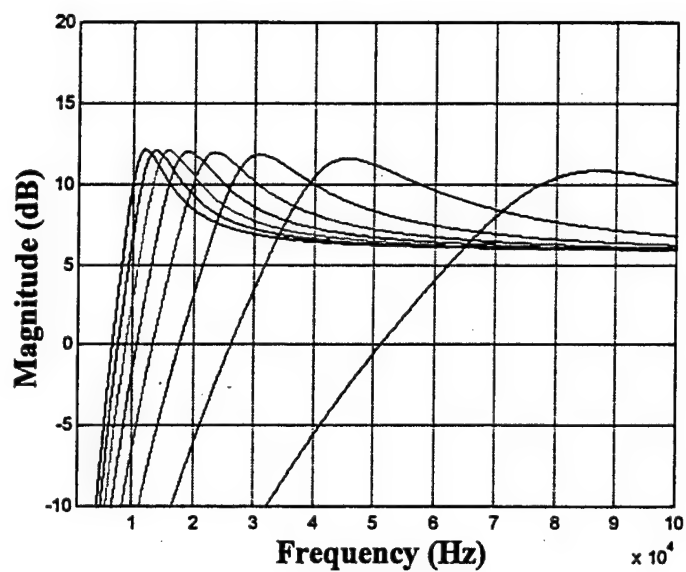
4. **High-Pass Filter, Quality Factor = 3, All Frequencies**
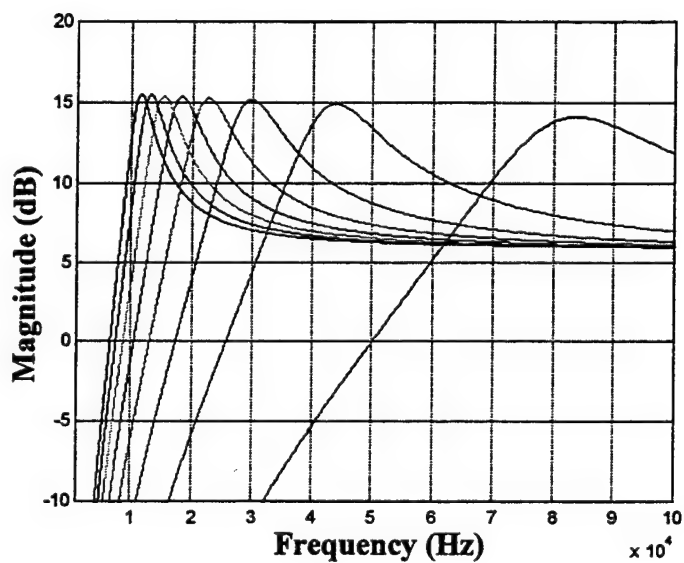
5. High-Pass Filter, Quality Factor = 4, All Frequencies
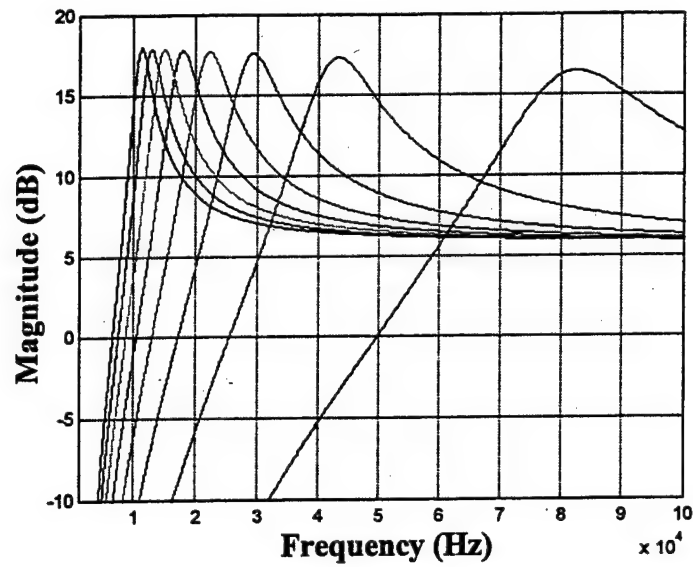
6. High-Pass Filter, Quality Factor = 5, All Frequencies
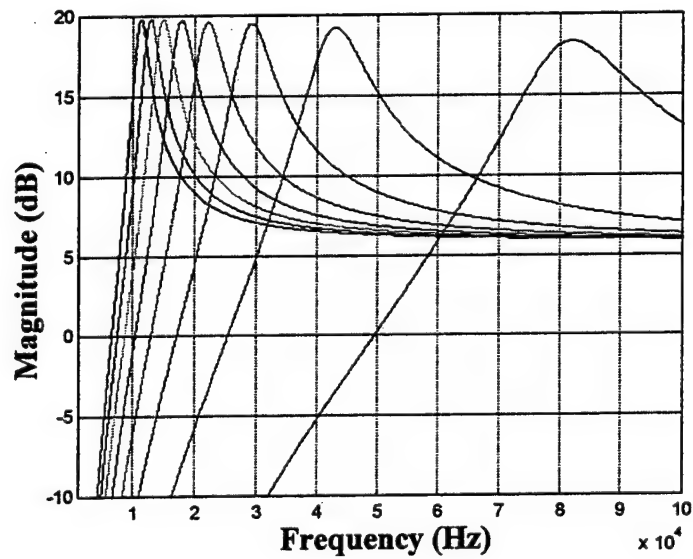
7. High-Pass Filter, Frequency = 90.00 kHz, All Quality Factors
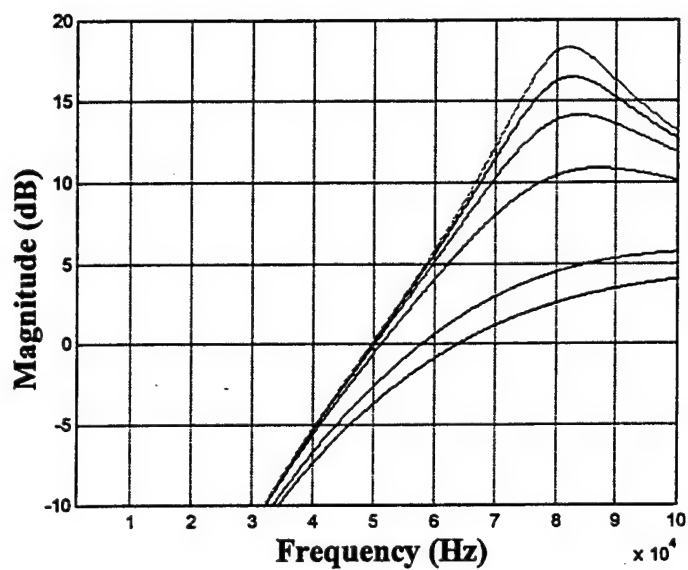
8. High-Pass Filter, Frequency = 51.60 kHz, All Quality Factors
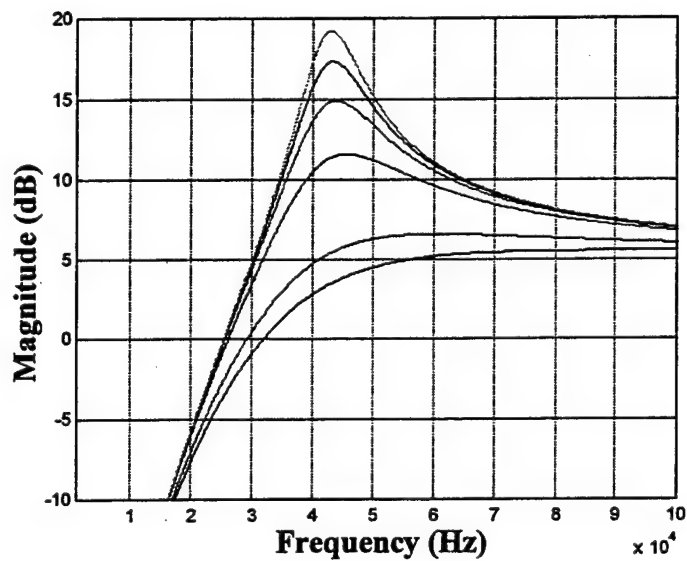
9. **High-Pass Filter, Frequency = 35.40 kHz, All Quality Factors**
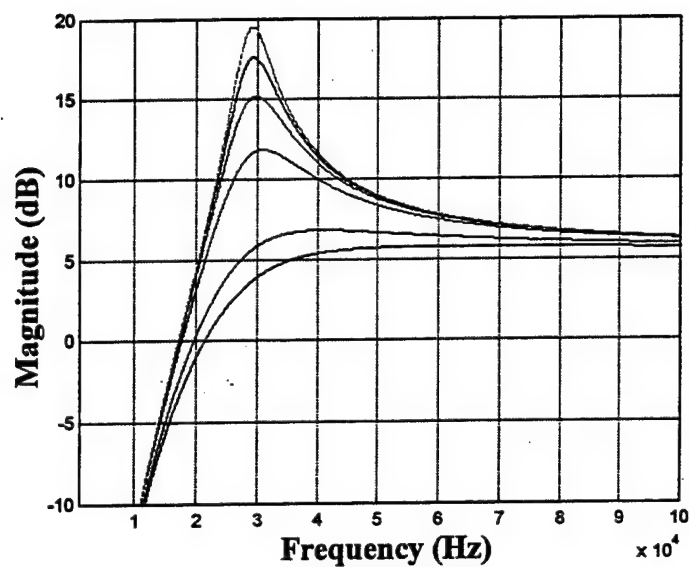
10. **High-Pass Filter, Frequency = 26.55 kHz, All Quality Factors**
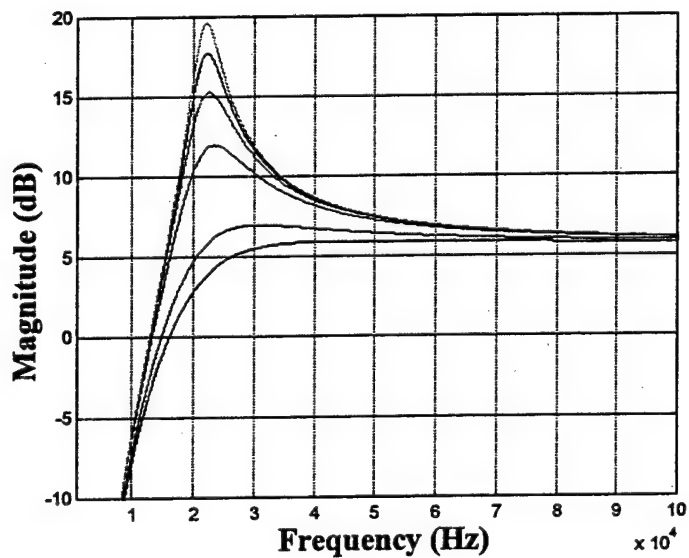
11. **High-Pass Filter, Frequency = 22.80 kHz, All Quality Factors**
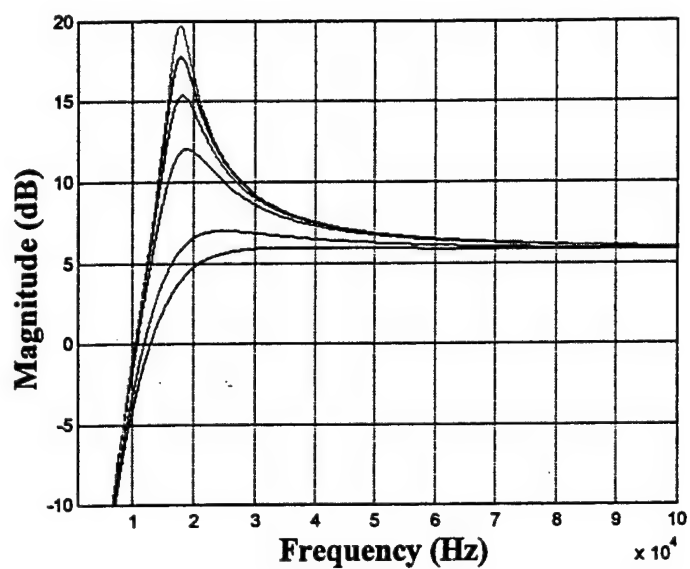
12. **High-Pass Filter, Frequency = 18.45 kHz, All Quality Factors**

103
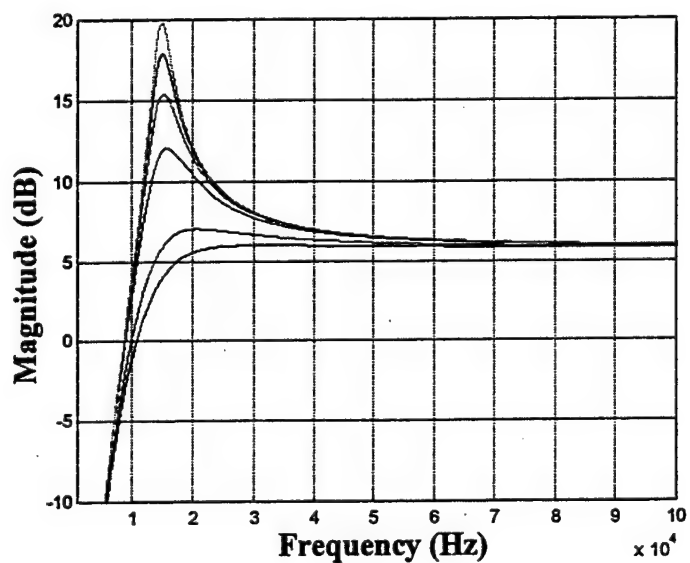
13.   High-Pass Filter, Frequency = 15.60 kHz, All Quality Factors
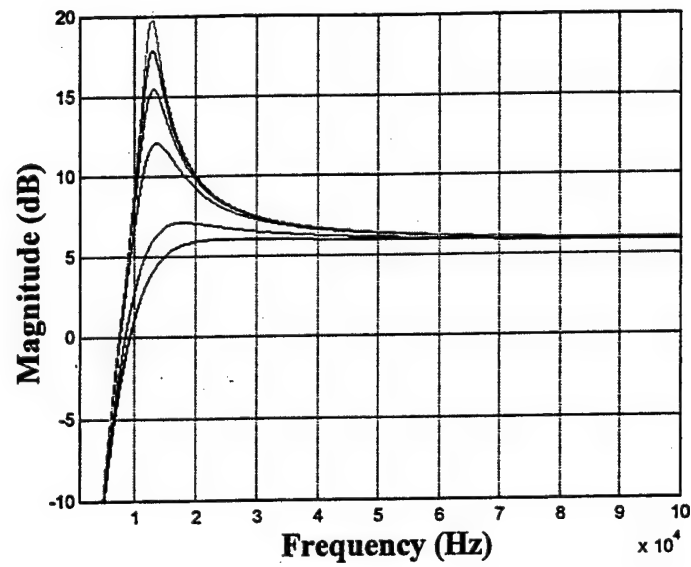
14.   High-Pass Filter, Frequency = 13.95 kHz, All Quality Factors
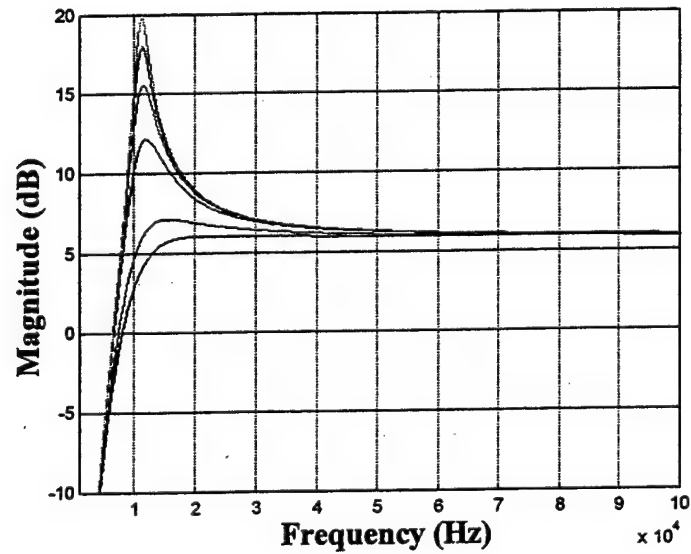
C.   BAND-PASS FILTERING

1.   Band-Pass Filter, Quality Factor = 0.8, All Frequencies
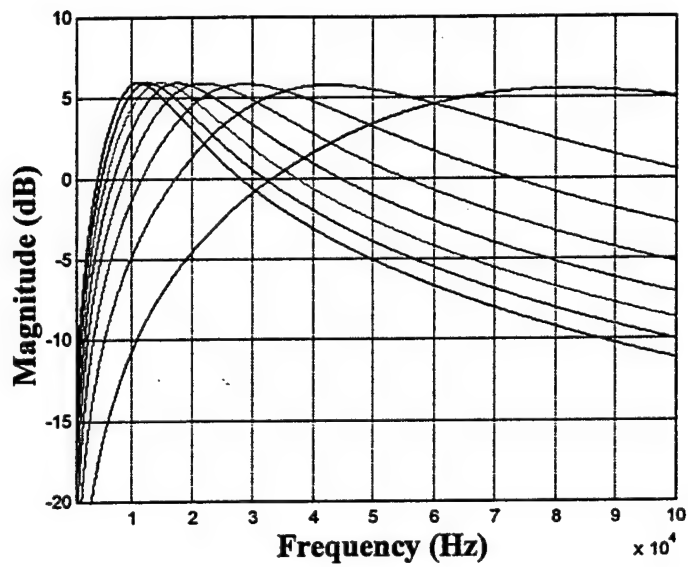
2.   Band-Pass Filter, Quality Factor = 1, All Frequencies
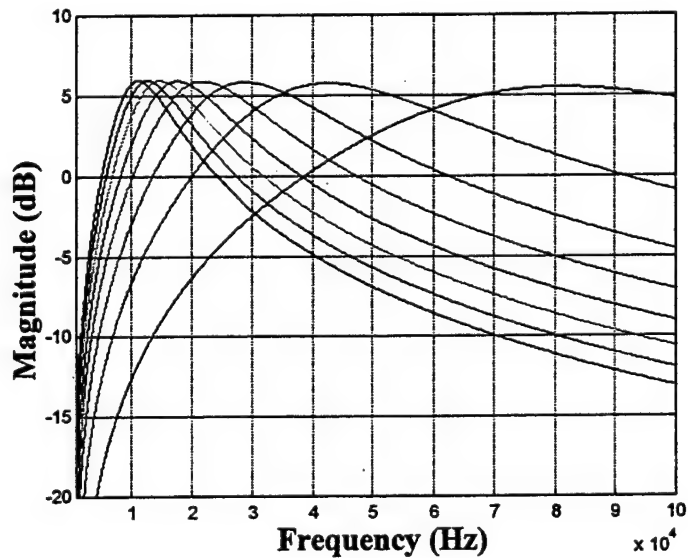
3.   Band-Pass Filter, Quality Factor = 2, All Frequencies
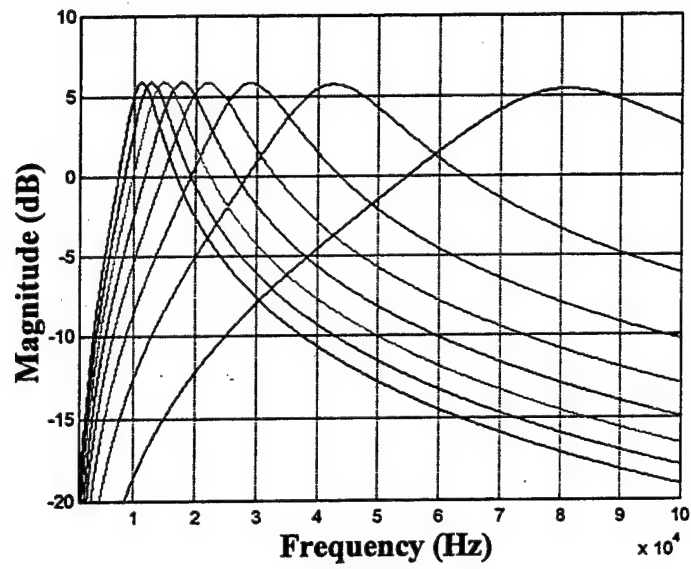
4.   Band-Pass Filter, Quality Factor = 3, All Frequencies
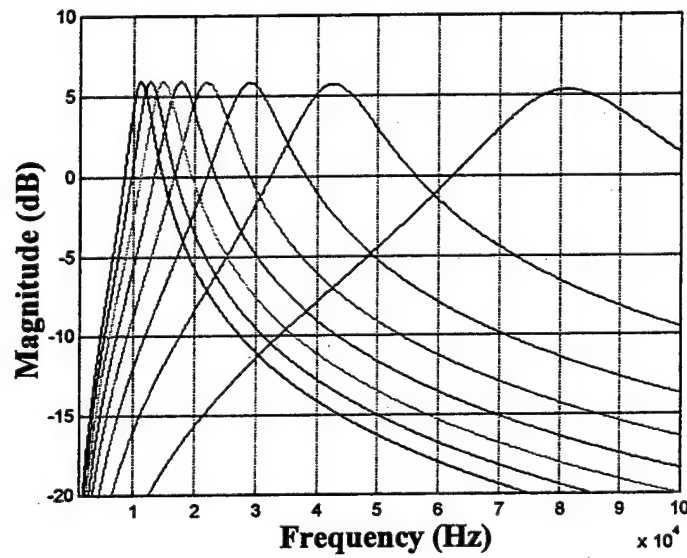
5.   Band-Pass Filter, Quality Factor = 4, All Frequencies
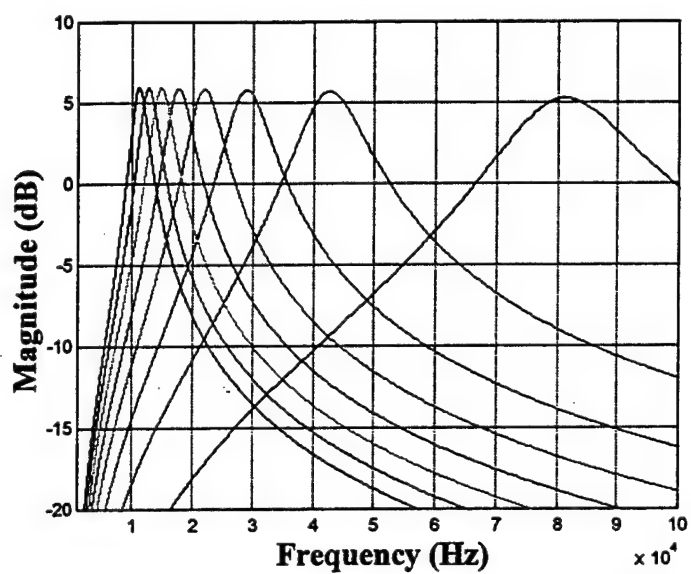
6.   Band-Pass Filter, Quality Factor = 5, All Frequencies

107
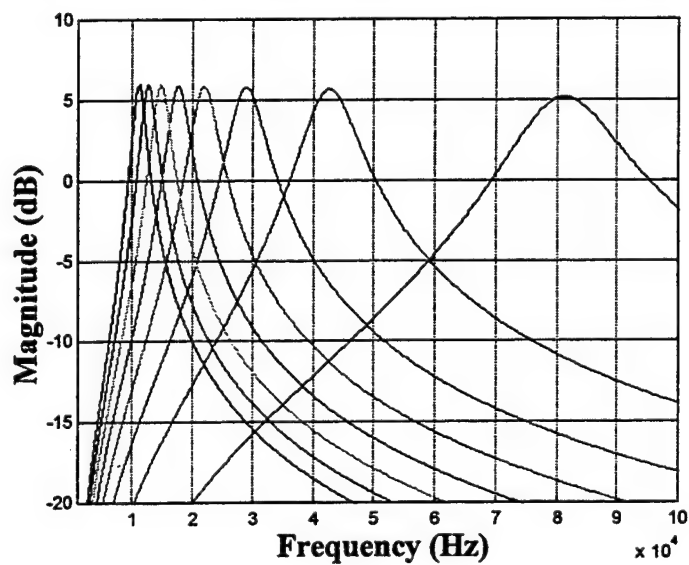
7.   Band-Pass Filter, Frequency = 90.00 kHz, All Quality Factors
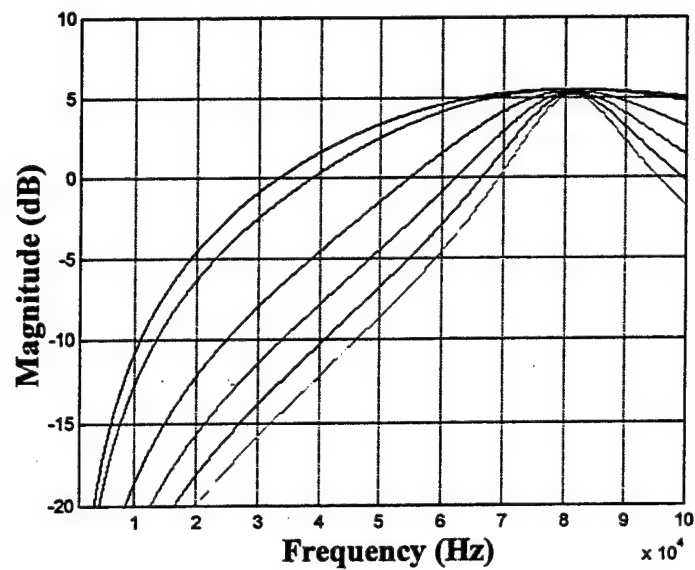
8.   Band-Pass Filter, Frequency = 51.60 kHz, All Quality Factors
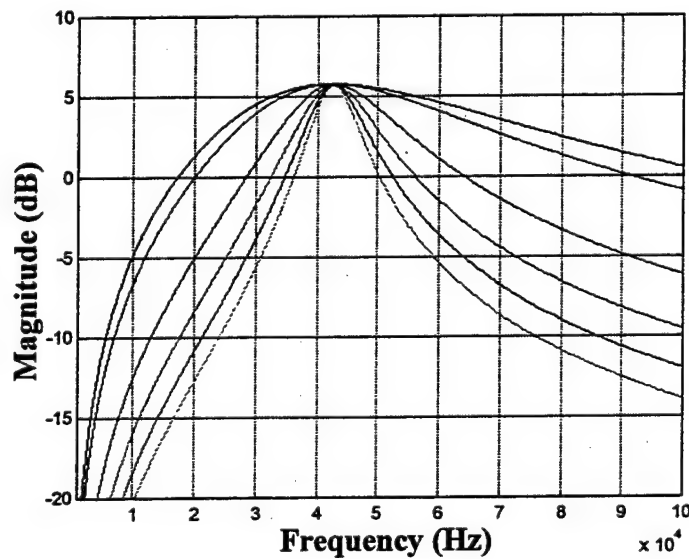
9. **Band-Pass Filter, Frequency = 35.40 kHz, All Quality Factors**
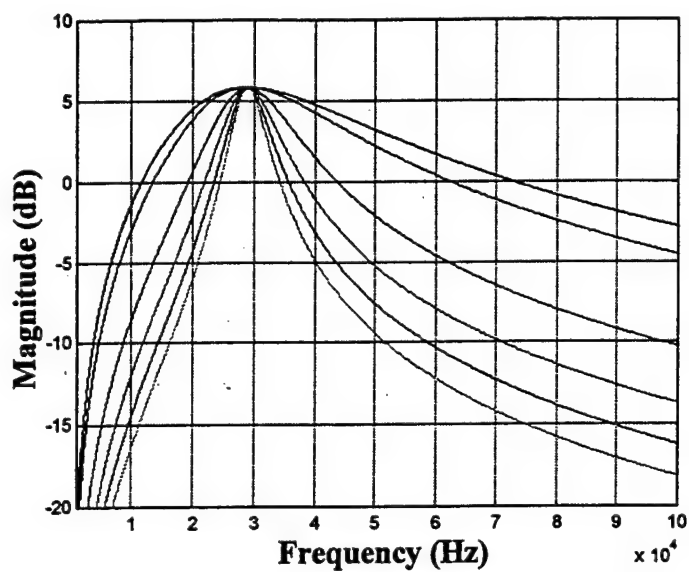
10. **Band-Pass Filter, Frequency = 26.55 kHz, All Quality Factors**
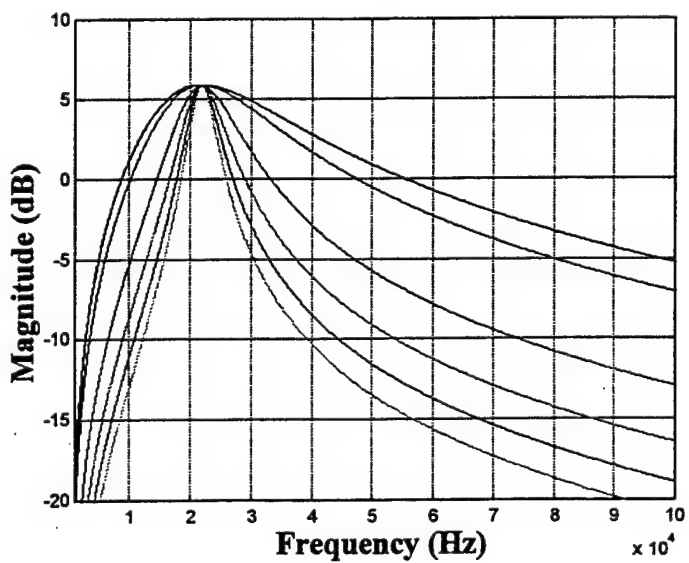
11. **Band-Pass Filter, Frequency = 22.80 kHz, All Quality Factors**
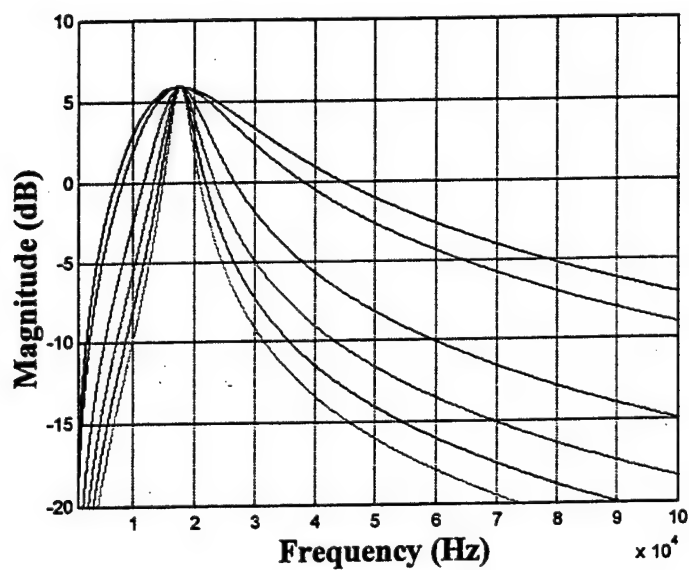
12. **Band-Pass Filter, Frequency = 18.45 kHz, All Quality Factors**

110
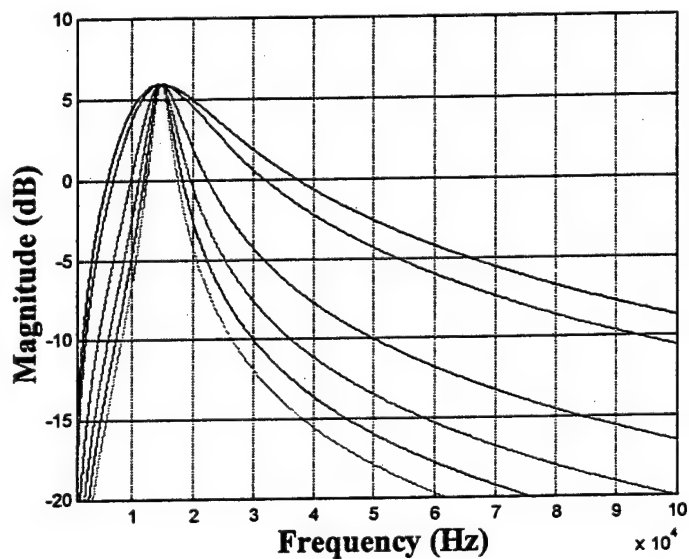
13.   Band-Pass Filter, Frequency = 15.60 kHz, All Quality Factors
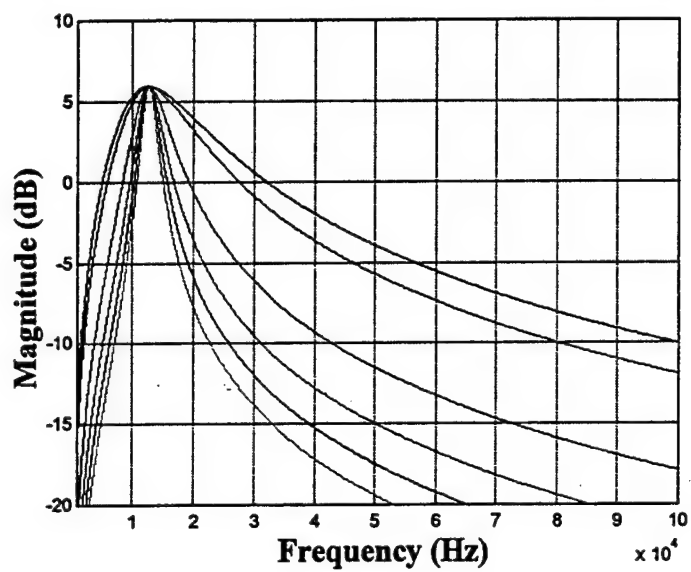
14.   Band-Pass Filter, Frequency = 13.95 kHz, All Quality Factors

111
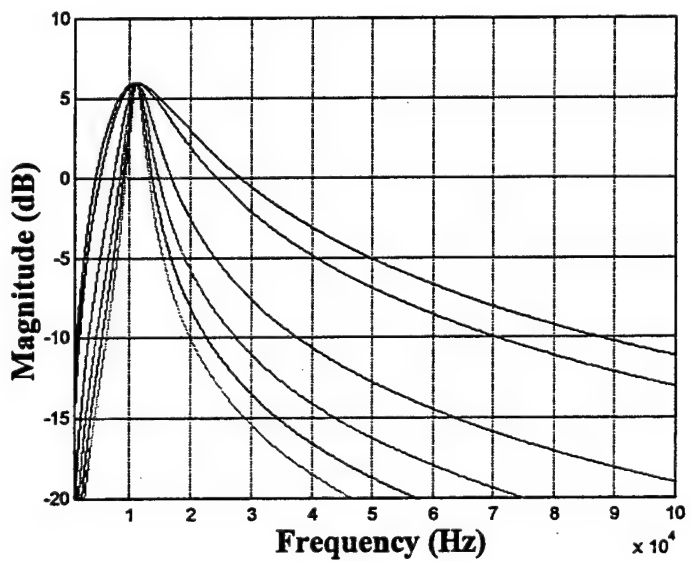
D.   NOTCH FILTERING

1.   Notch Filter, Quality Factor = 0.8, All Frequencies
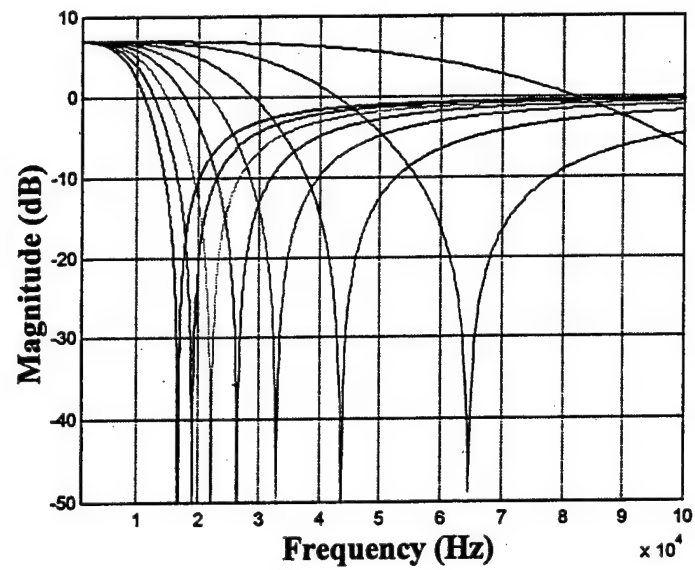
2.   Notch Filter, Quality Factor = 1, All Frequencies

112
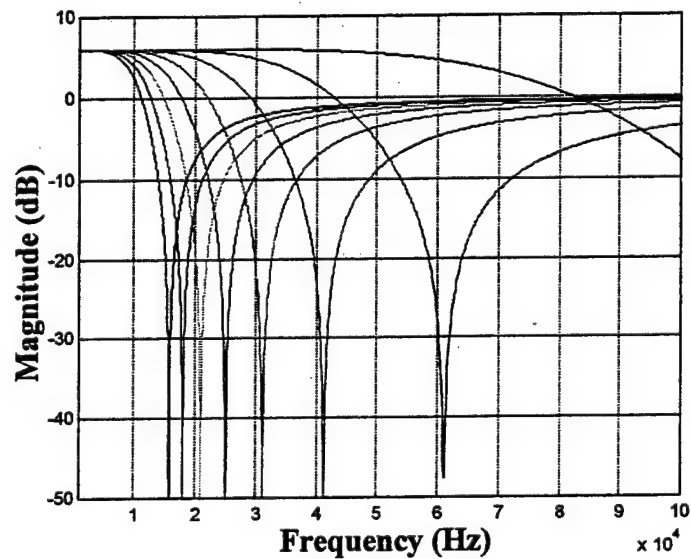
3.   Notch Filter, Quality Factor = 2, All Frequencies
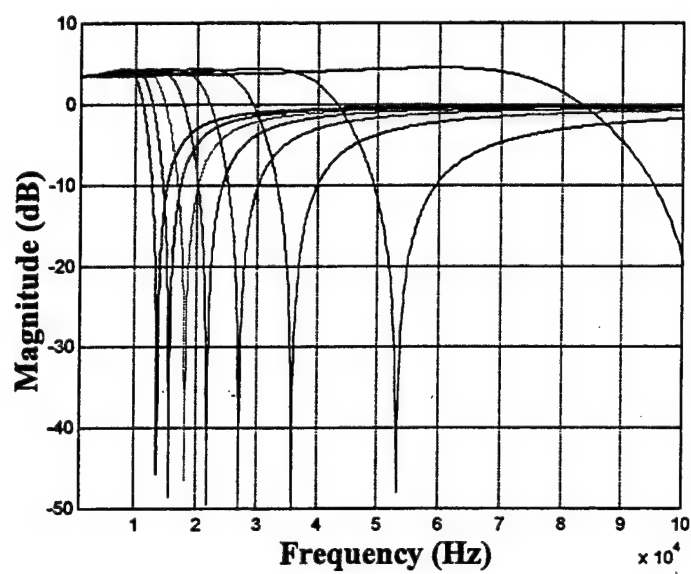
4.   Notch Filter, Quality Factor = 3, All Frequencies

113
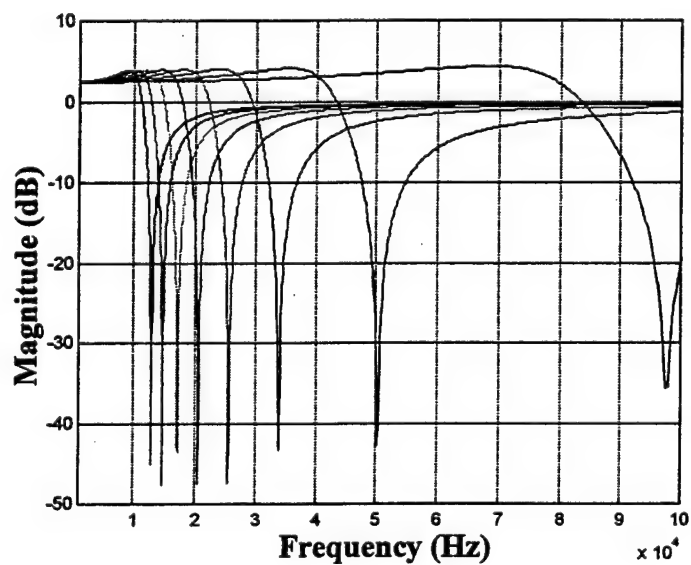
5. **Notch Filter, Quality Factor = 4, All Frequencies**
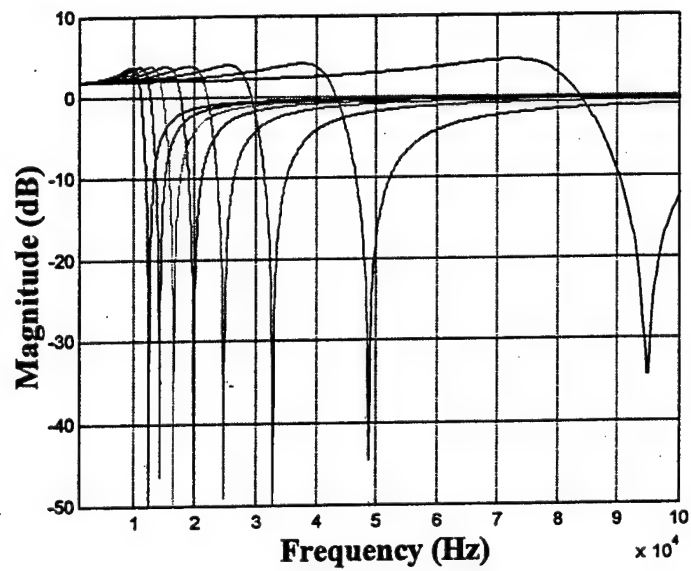
6. **Notch Filter, Quality Factor = 5, All Frequencies**

114
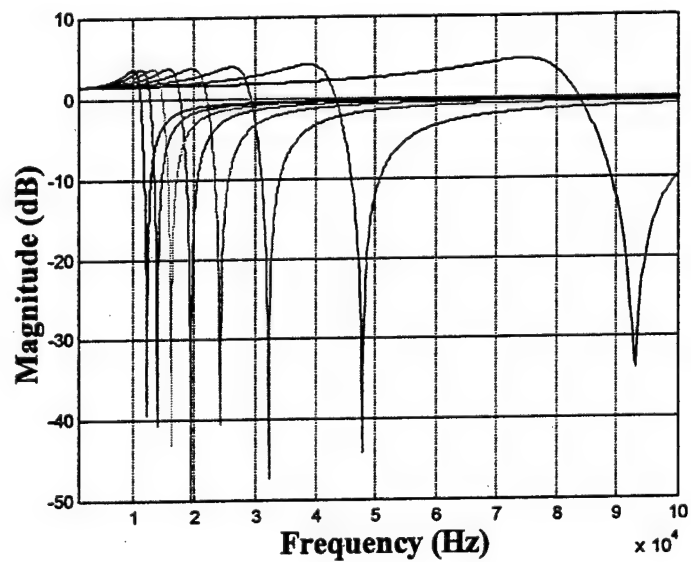
7. **Notch Filter, Frequency = 90.00 kHz, All Quality Factors**
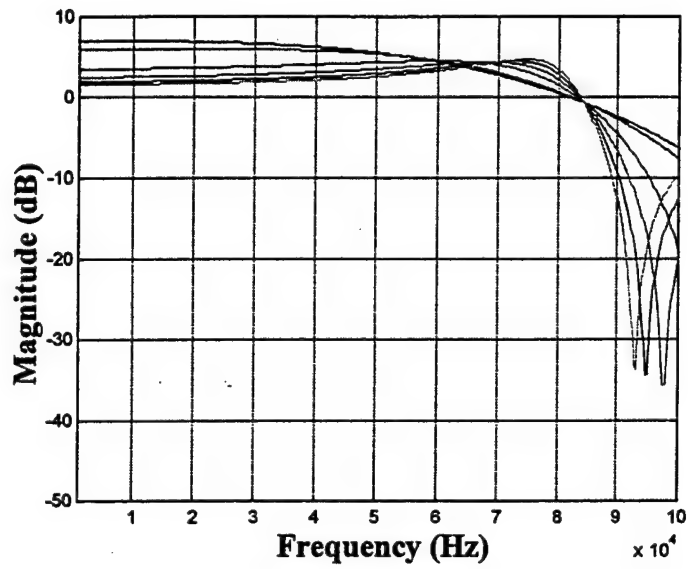
8. **Notch Filter, Frequency = 51.60 kHz, All Quality Factors**
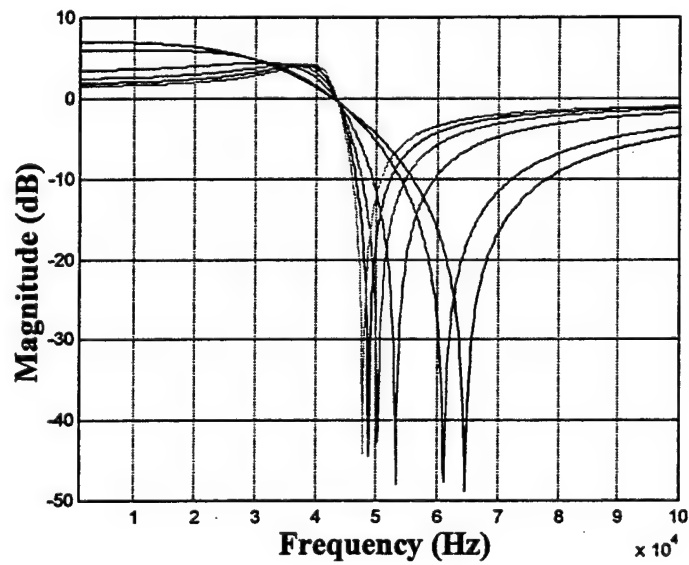
9. **Notch Filter, Frequency = 35.40 kHz, All Quality Factors**
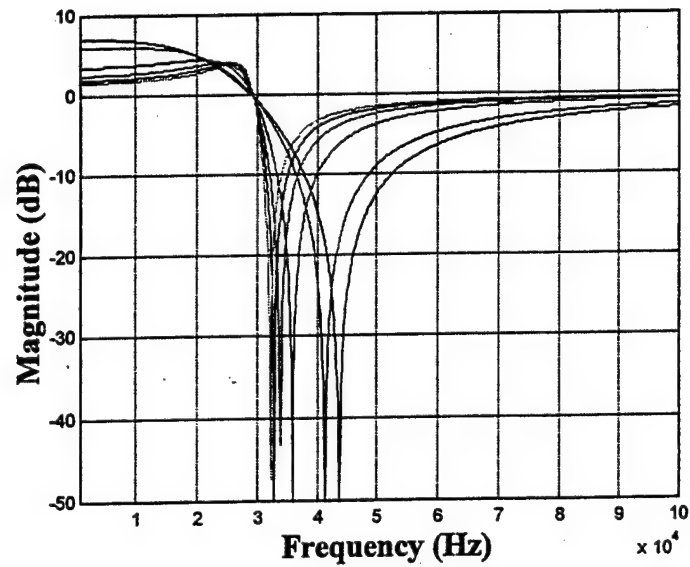
10. **Notch Filter, Frequency = 26.55 kHz, All Quality Factors**
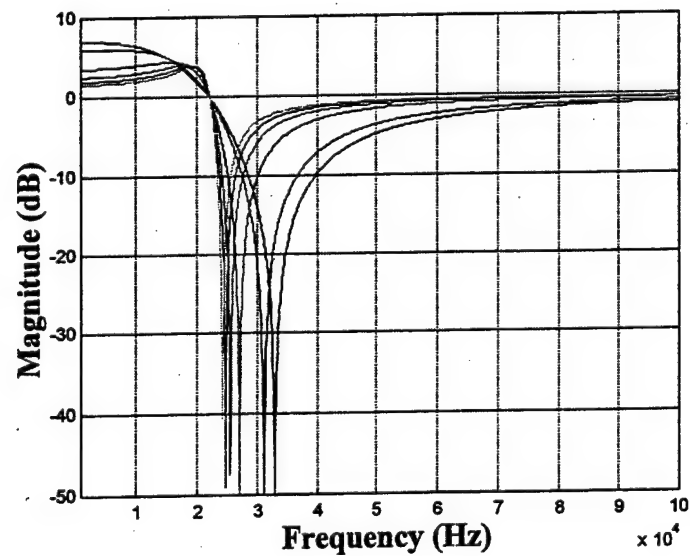
11. Notch Filter, Frequency = 22.80 kHz, All Quality Factors
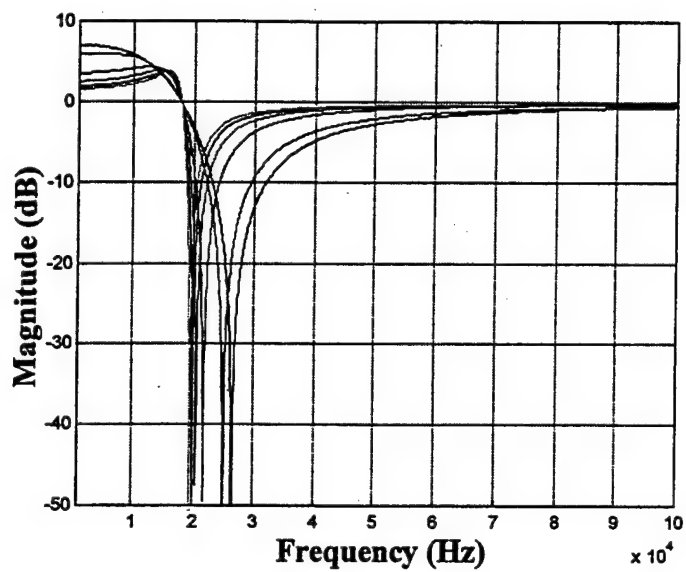
12. Notch Filter, Frequency = 18.45 kHz, All Quality Factors
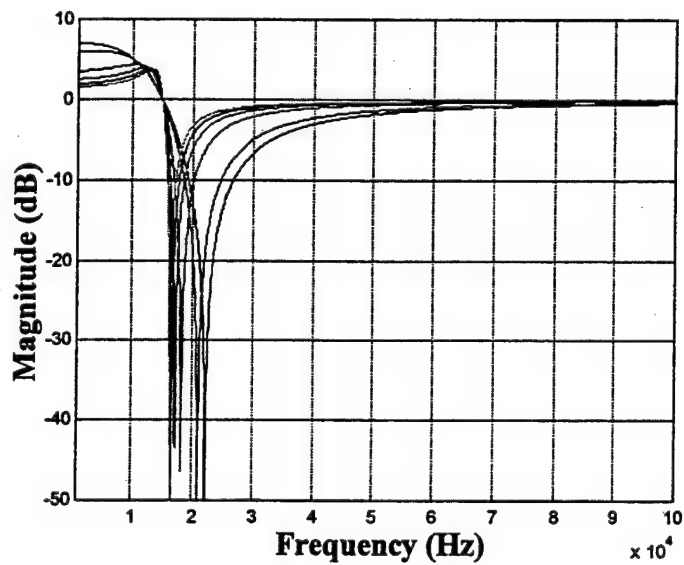
13.   Notch Filter, Frequency = 15.60 kHz, All Quality Factors
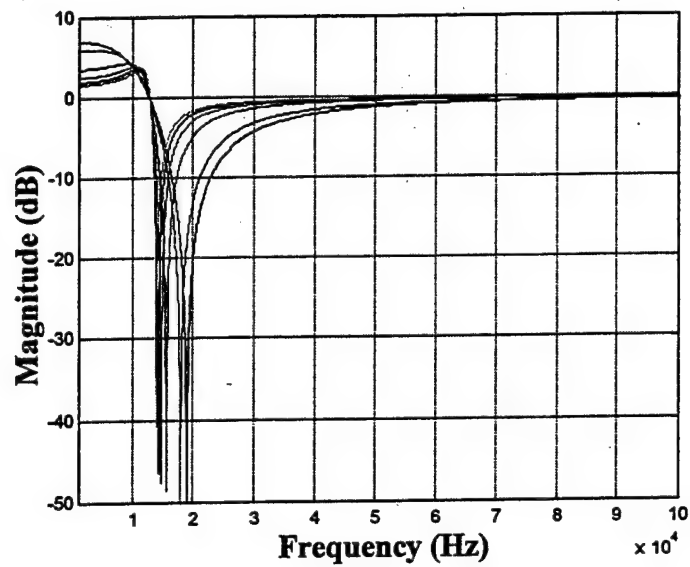
14.   Notch Filter, Frequency = 13.95 kHz, All Quality Factors
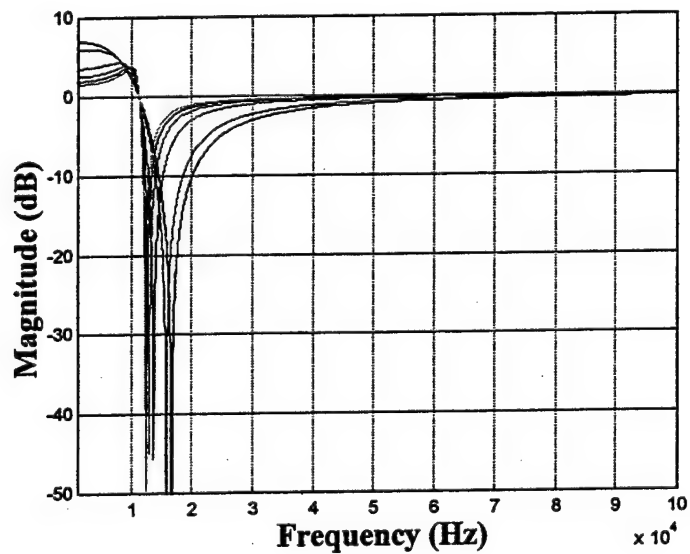
APPENDIX B. VLSI LAYOUTS

A.   LOGIC INVERTER – (INV_LOG)
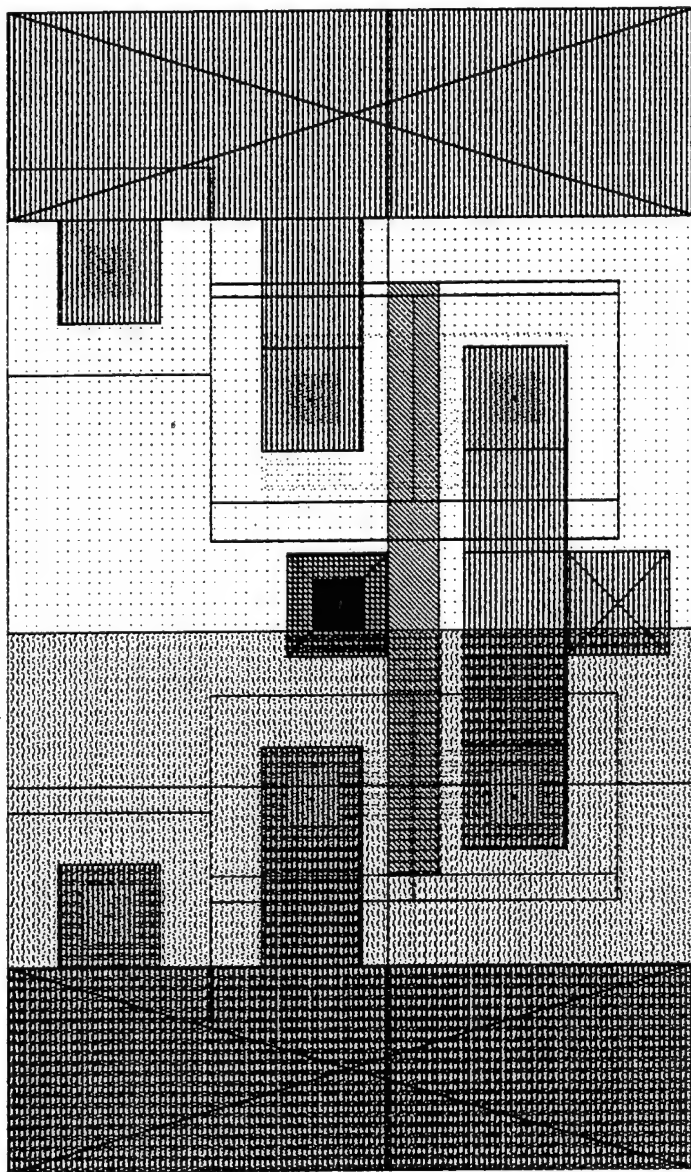
B. **INVERTER C1 – (INV_C1)**
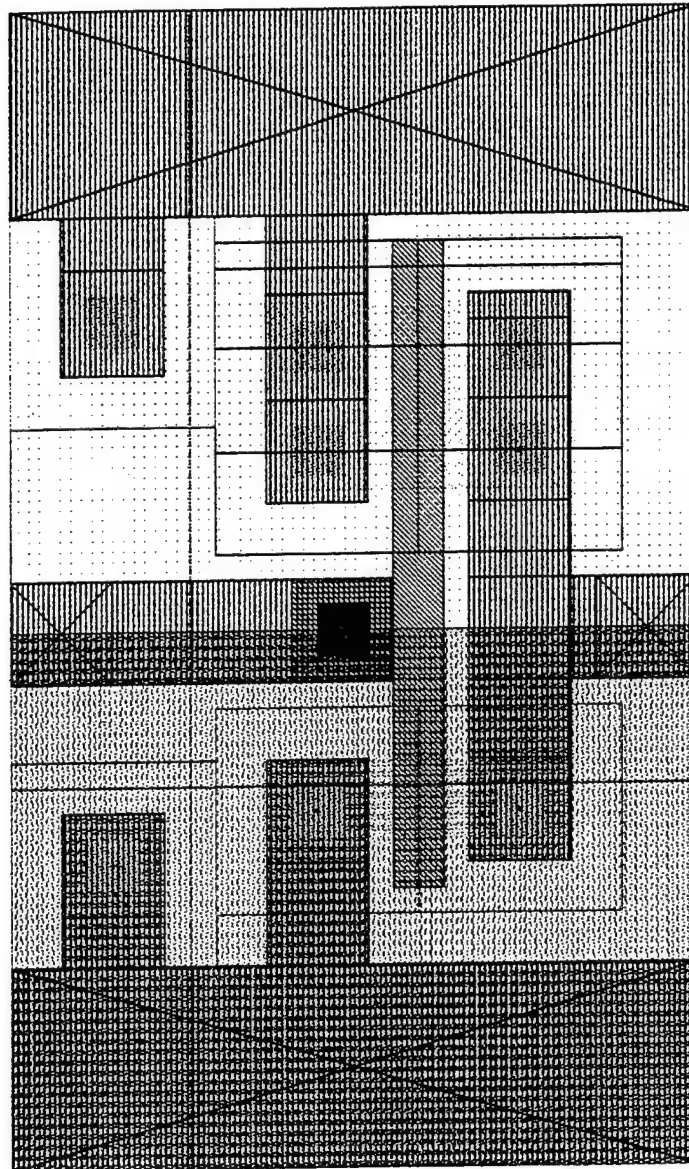
C. INVERTER C2 – (INV_C2)
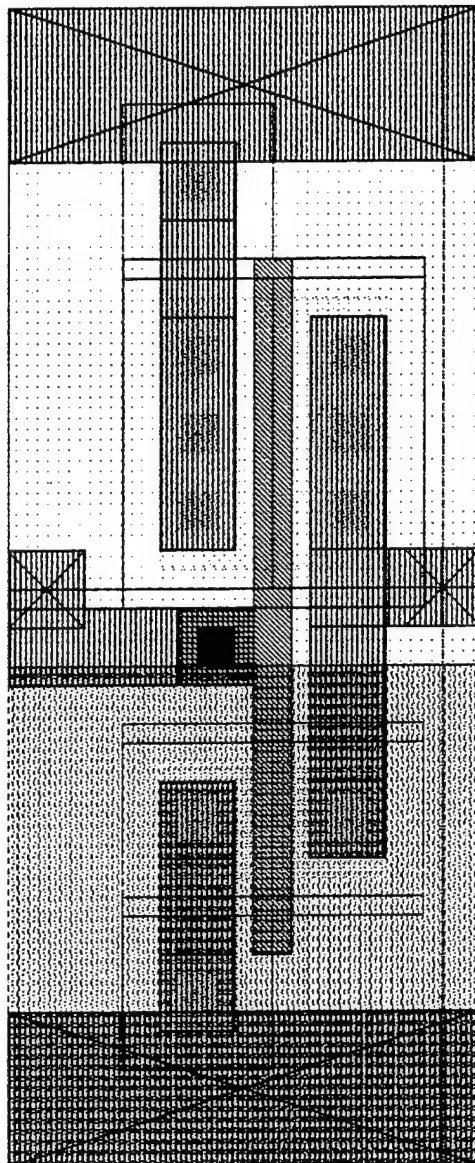
D.   **INVERTER C3 – (INV_C3)**

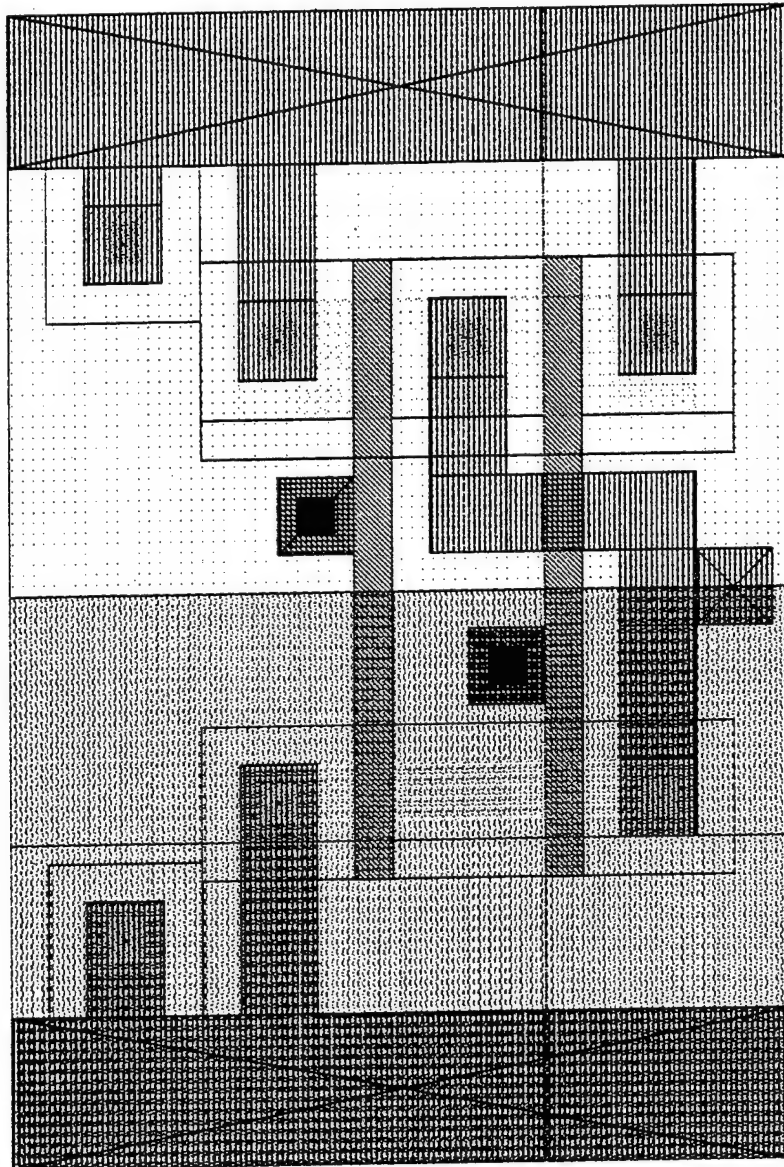# E. PASSGATE

123
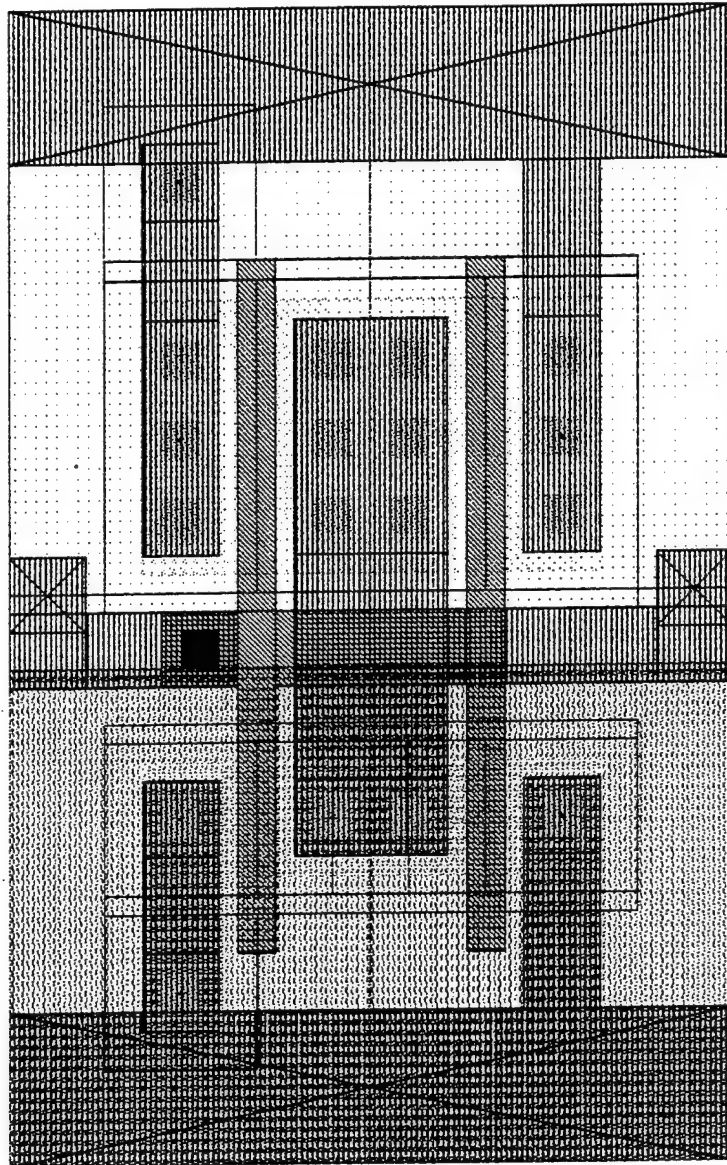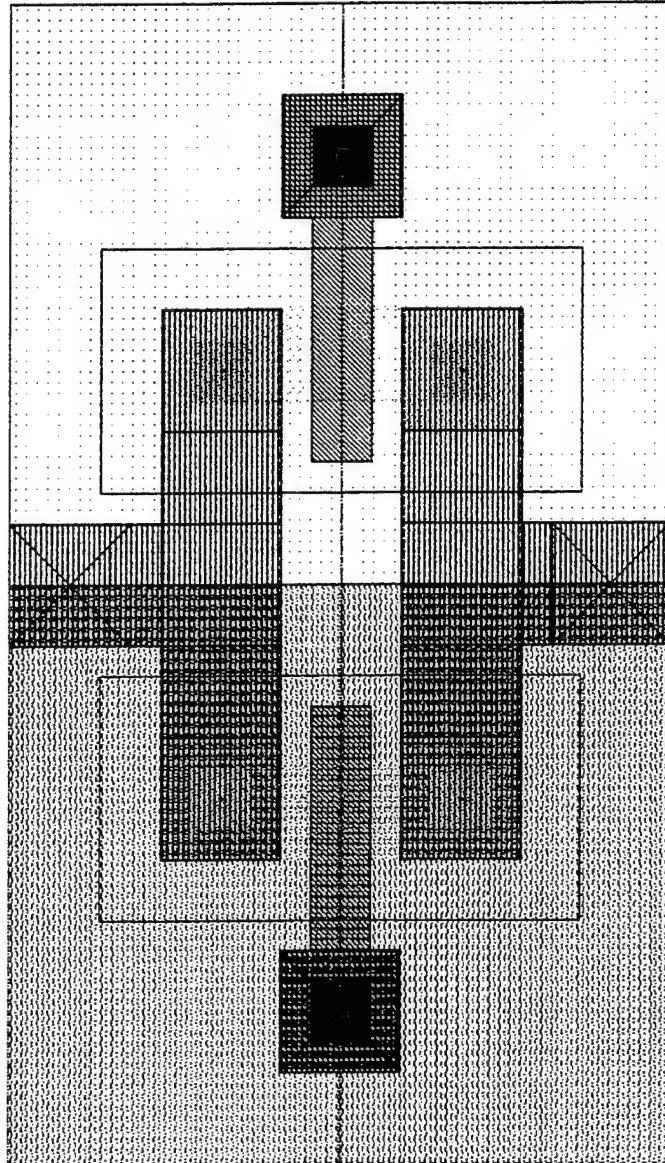
F.   SINGLE INPUT PASSGATE – (PASSGATE_SI)
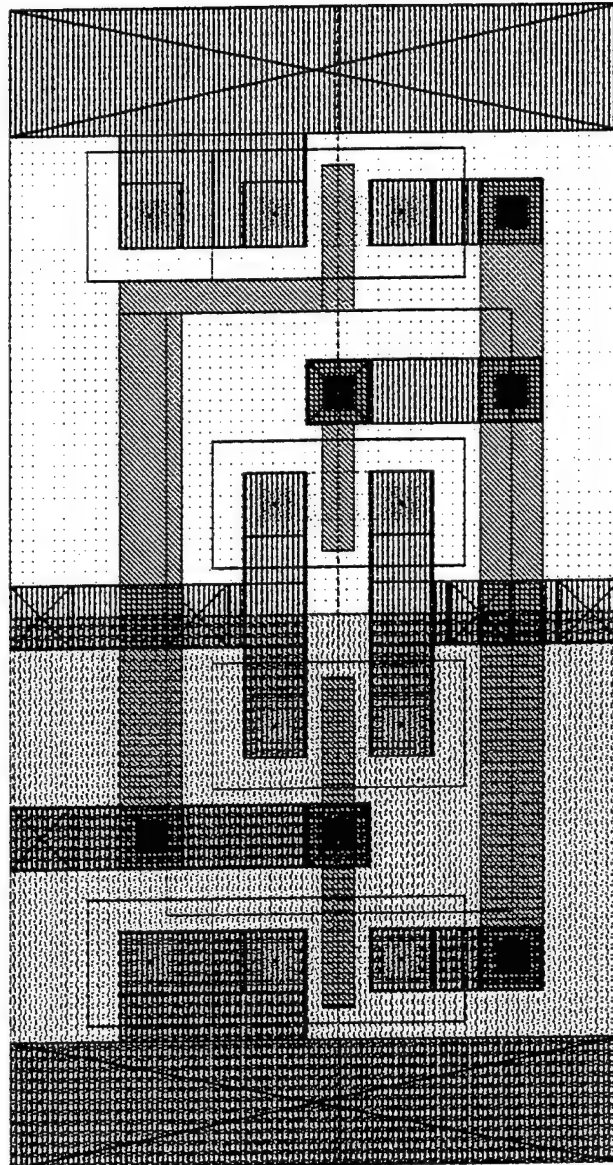
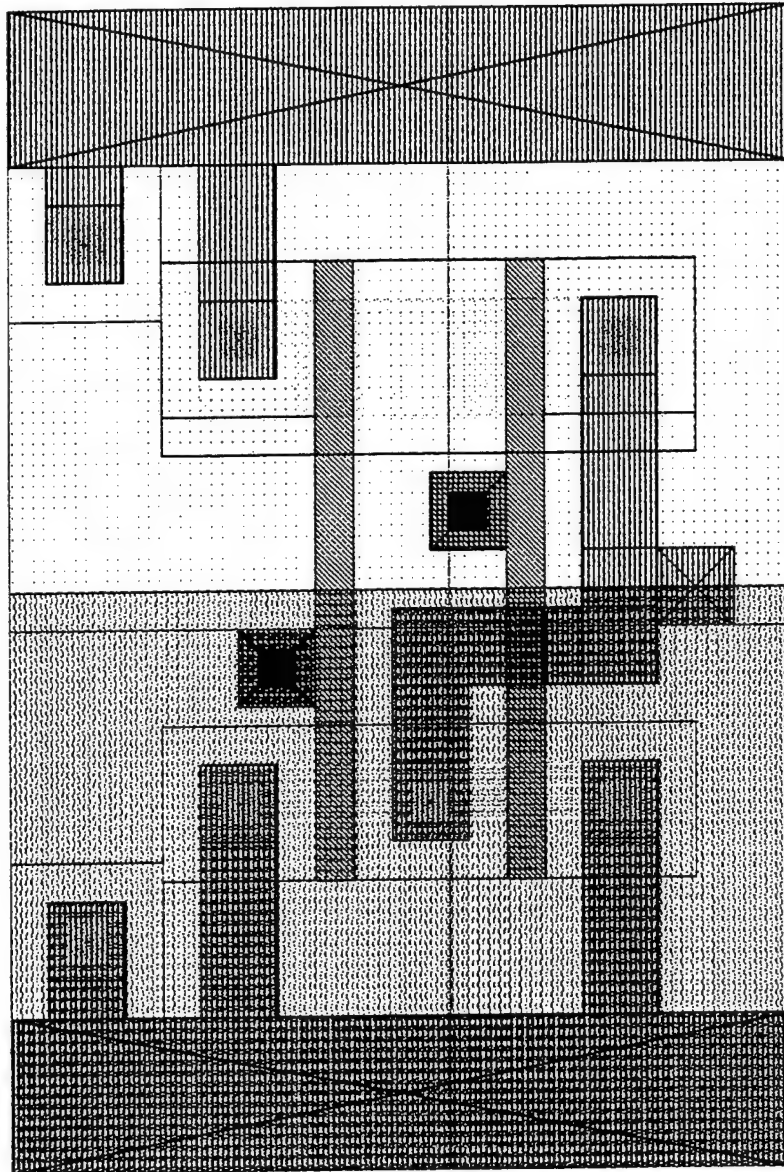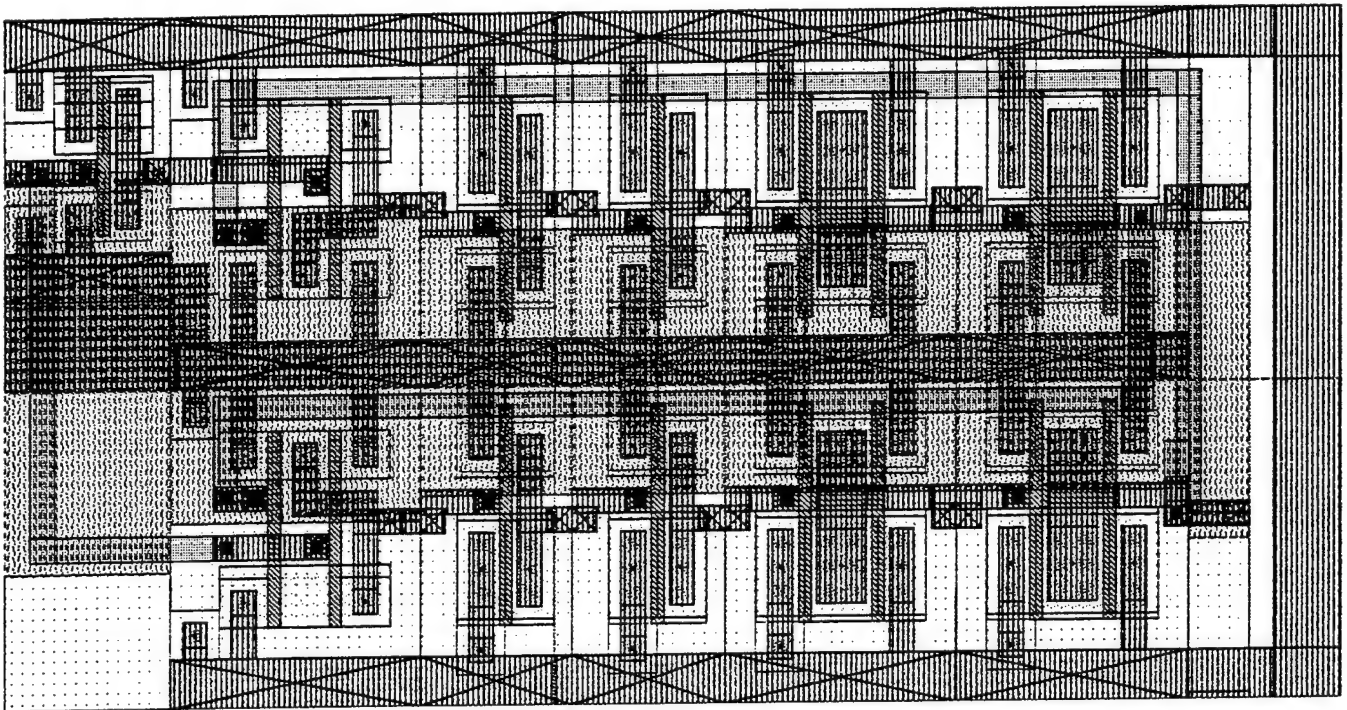## G. BUFFER
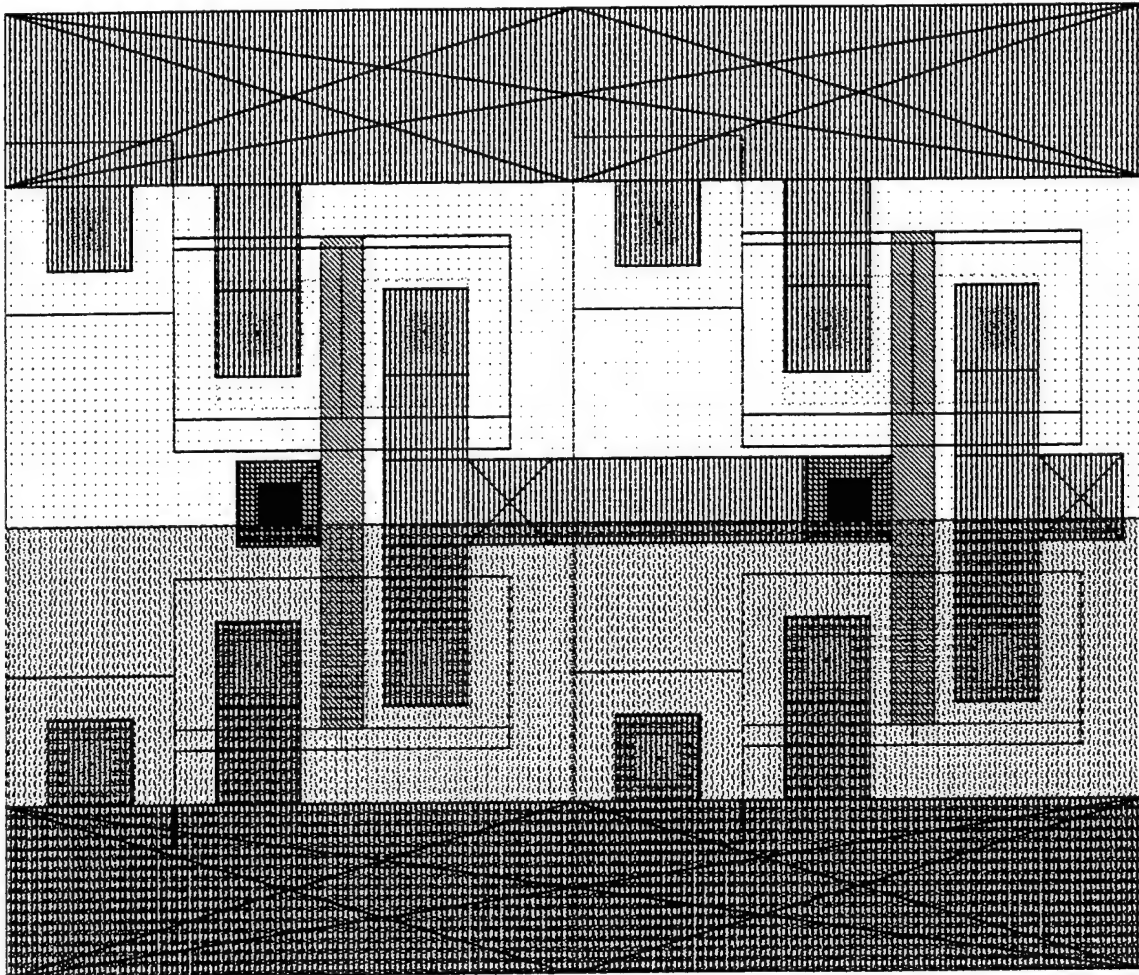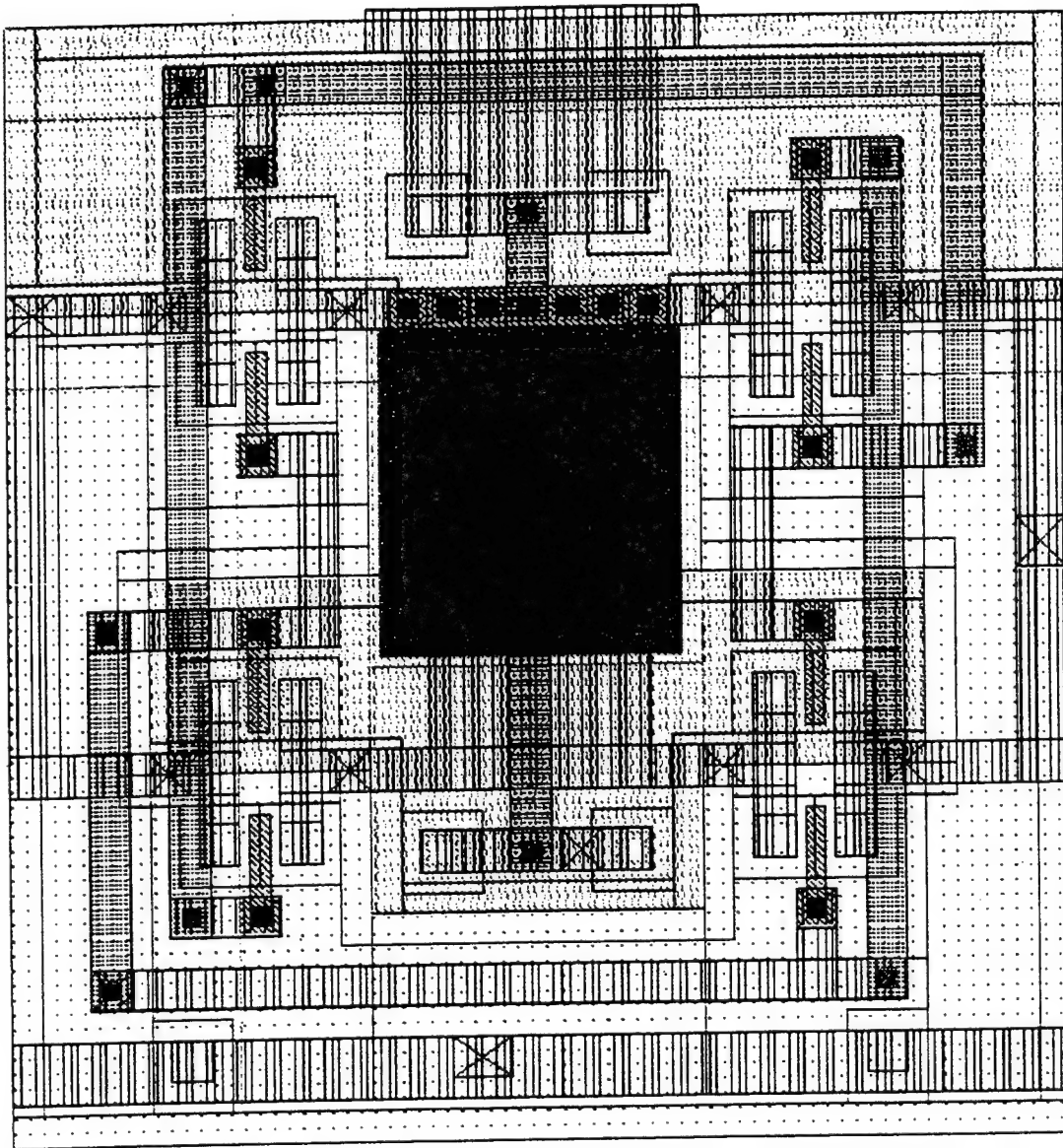
H. TWO INPUT NAND GATE – (NAND2)

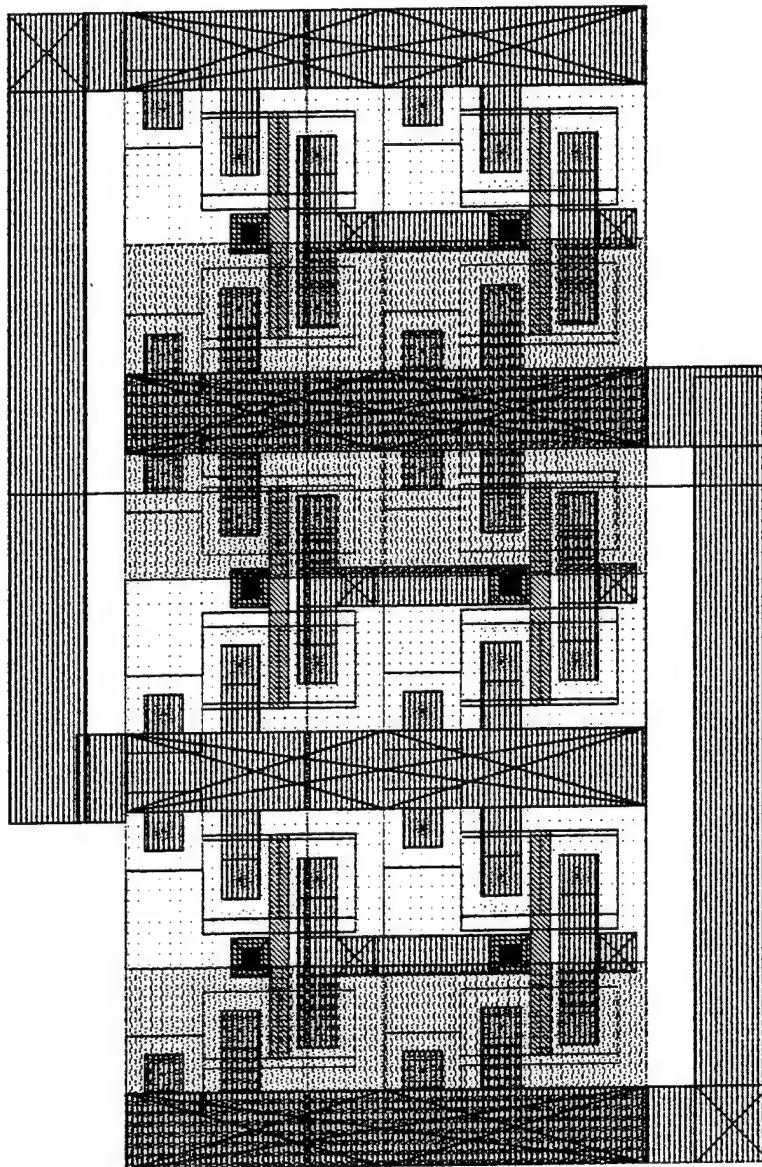# I.   TWO INPUT NOR GATE – (NOR2)

J. TWO PHASE CLOCK

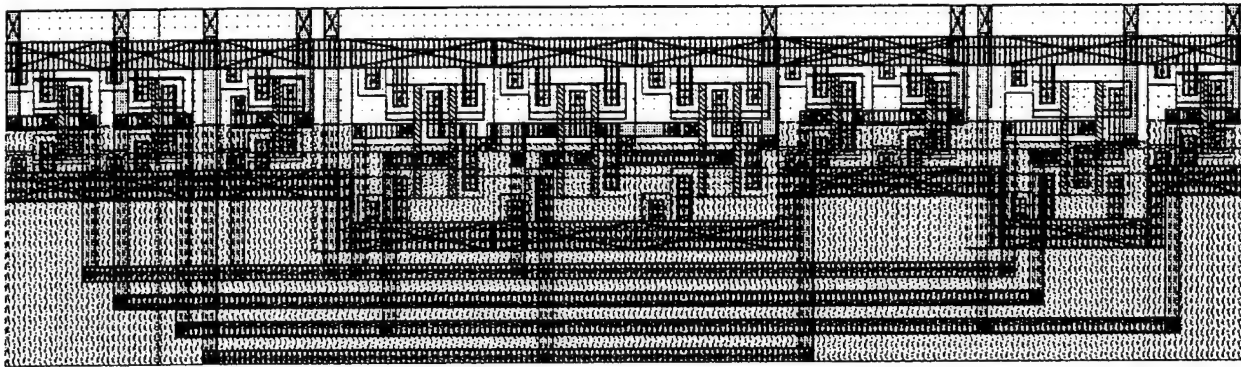## K.   BILINEAR SWITCHED CAPACITOR (FLOATING BILINEAR RESISTOR)

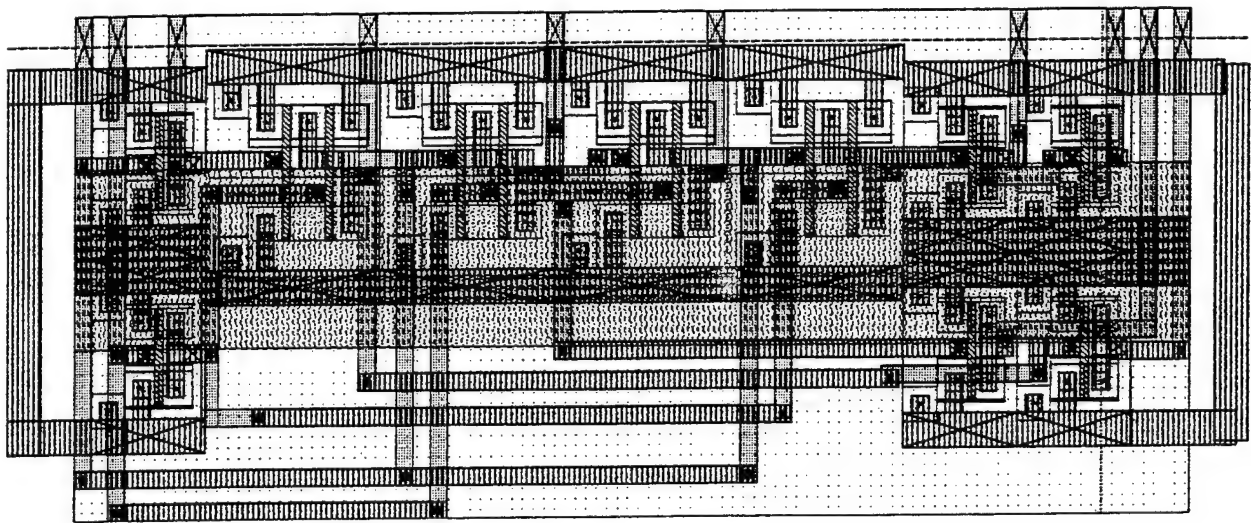

[Ref. 7]

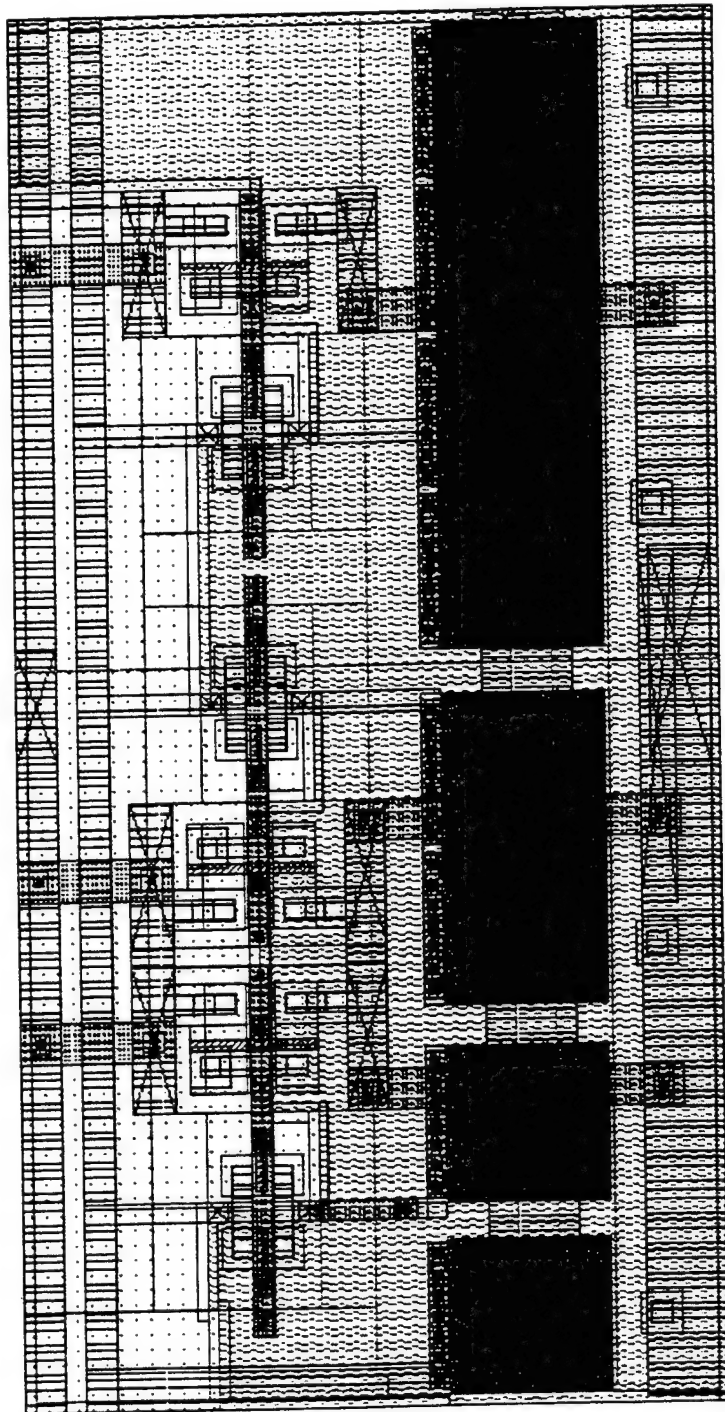**L.** **FREQUENCY SELECTION LOGIC**

M. QUALITY FACTOR SELECTION LOGIC

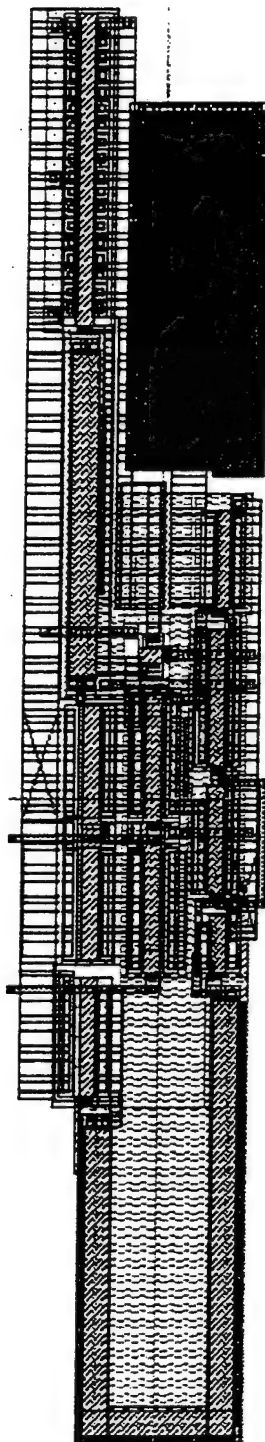# N. TOPOLOGY SELECTION LOGIC

O.   VARIABLE CAPACITOR

[Ref. 7]

P.   OP AMP

[Ref. 9]

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